PERFORMANCE ANALYSIS OF ALL-OPTICAL PACKET SWITCH WITH HEADER REPLACEMENT MECHANISM

A Thesis submitted
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by
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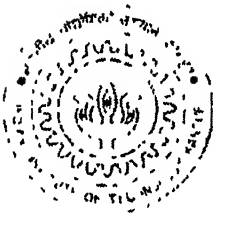

to the
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CERTIFICATE

This is to certify that the work contained in this M Tech thesis titled ***PERFORMANCE ANALYSIS OF ALL-OPTICAL PACKET SWITCH WITH HEADER REPLACEMENT MECHANISM*** *has been carried out by* **PANKAJ DWIVEDI** *under my supervision and has not been submitted elsewhere for any degree or diploma*

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Dedicated to

My Parents and Grand Parents

Abstract

Photonic technology has capability to fulfill increasing demand of the telecommunication services in the near future. The electronic header replacement in Optical Switches has been the main hitch in optimum use of this technology. Several efforts are being made to avoid the use of electronic header replacement and go for optical header replacement resulting into development of all-optical switches. In all kind of switches the header replacement is done before the actual switching.

In this thesis, we conducted a survey on methods of optical header replacement. Further, as an innovative approach, we propose the integration of header replacement and switching. For this purpose a method of header replacement based on two SOAs connected in parallel, and a WDM switch based on Fiber Optical Loop Memory (FOLM) has been considered. The proposed scheme leads to saving of an SOA for each channel, but the minimum delay of the packet in the switch increases. Using the computational models of different components of loop, the noise analysis of the proposed scheme is done. It leads to the conclusion that the proposed scheme can not be used efficiently for 5 or more channels because in this case maximum 5 rotations are allowed in the loop. Also in case of different input powers to different channels at a time, the channel with least input power has lowest SNR and if this input power is too low then signal will have to be rejected due to low SNR.

Acknowledgement

I would like to express my sincere gratitude to my thesis supervisor Dr. Y. N Singh for his help during my M Tech Thesis and for giving me complete freedom in choosing the thesis problem. Under his kind guidance I learned how to investigate and learn in new field of knowledge He was always available to help, guide and encourage me. No words can be said for his tolerance and cooperation during thesis work.

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Words are not enough to express my feelings towards my family members. My Parents and Grandfather always stood by my side to give me spiritual and mental strength in my all endeavors.

Pankaj

Contents

List of Figures

List of Tables

Chapter 1

Introduction

In the near future the demand for various kind of telecommunication services is bound to increase. These services have different quality requirement depending upon their nature. The Idea to provide them through a single network is resulting into development of Broadband Integrated Services Digital Network (BISDN). Main requirements for BISDN are wide bandwidth, high speed and fast switching which are difficult to meet with electronic technology. Photonic technology has capability to fulfill these requirements and presently numerous efforts are being made to exploit it.

Optical fiber has already replaced cables as transmission media for the most of the long distance (Wide Area Network (WAN)) as well as short distance (Metropolitan Area Network (MAN), Local Area Network (LAN)) networks. But at switching nodes still the electronic technology is being used. Optical to electrical and electrical to optical conversion at ultra high bit rate ($\geq 10 Gbps$) is difficult. Therefore optical switching is attractive. Use of optical switching will make it possible to have ultra high bit rates in optical fiber, thereby utilising the available capacity. Hence a lot of work is being done to develop all-optical switching techniques.

1.1 Different Kind of Switching

There are three kind of switching namely circuit switching, packet switching and message switching [1] The third one viz message switching can be put with packet switching because the messages are generally broken into small packets so that the bandwidth can be used efficiently

1.1.1 Circuit Switching

In this scheme the end to end physical path is established between designated users There are three phases in this scheme The connect phase in which the path is established the traffic phase in which payload data is sent and disconnect phase in which the path is de-established Here during traffic phase there may be instants when no information is being transmitted. These instances are known as dead time As shown in Figure 1 1 in this scheme the call requests are usually queued at a single switch controller When queue gets filled the incoming calls are lost Thus it has a nonzero blocking probability An example is POTS (Plain Old Telephone Services)

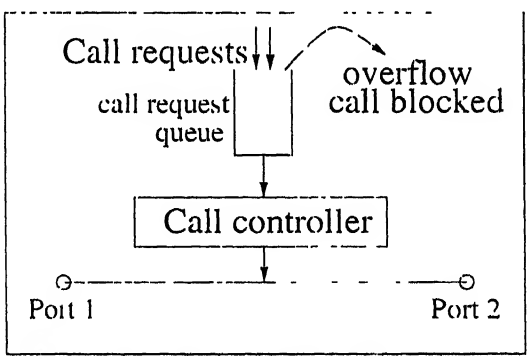


Figure 1 1 Circuit Switching

1.1.2 Packet Switching

In packet switching information to be transmitted is broken down into packets. Each packet is provided with a header. Each packet is independently transported to destination using the information provided in the header. The intermediate nodes use the header information and switch the packet to appropriate output. Each link in packet switched network may be shared across many concurrent connections connecting to different places. Thus packet switching is not protocol transparent while the circuit switching is. Here also packets are queued up in buffers at each node. Due to finite size of buffer, there is always a nonzero probability of packet loss at each buffer. Packet switching is most suitable for BISDN, because information from different sources can be broken into packets and transmitted. This gives efficient utilization of available bandwidth.

1.2 Asynchronous Transfer Mode (ATM)

ATM is widely accepted as a key component of BISDN. It provides technical capability to handle any kind of information voice, video, data and text in an integrated manner. It is a connection oriented fast packet switching technique. The information is organised in fixed length packets called cells which consists of a header and user information field. The small cell size reduces the packetisation delay and also provides high flexibility for effective use of bandwidth. Further the fixed cell size reduces the switch design complexity [2].

The transfer mode used in ATM network is asynchronous mode i.e. ATM uses asynchronous time division multiplexing. Asynchronous TDM achieves high throughput and efficiency by statistically multiplexing cells belonging to different connections. The basic transport structure in ATM is synchronous. Therefore each link carries the slots. These slots are occupied by cells synchronously.

Some advantages of ATM are

- In ATM there is no separate signalling channel as required in circuit switched networks
- This provides flexibility in accommodation of diverse applications
- Small fixed size cell also makes it possible to control delay for delay sensitive services

1.2.1 ATM Cell Structure

An ATM cell has 53 bytes. Of these 5 bytes are used for header and 48 bytes are used for information payload [3]. Header contains many information fields based upon which cell is switched in network.

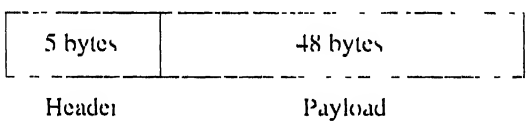


Figure 1.2: Cell Structure

1.2.1.1 ATM Header Structure

The design of cell header in packet switching is important as it governs routing and switching of packet in network. Since switching in ATM has to be performed in lower layers using hardware, ATM uses very simple header design. The structure of ATM header is shown in Figure 1.3 [3].

Various field in ATM header are as follows:

- Generic Flow Control (GFC): This is 4 bit field, present only at User Network Interface (UNI). It is used to arbitrate usage between multiple terminals sharing the same physical connection.

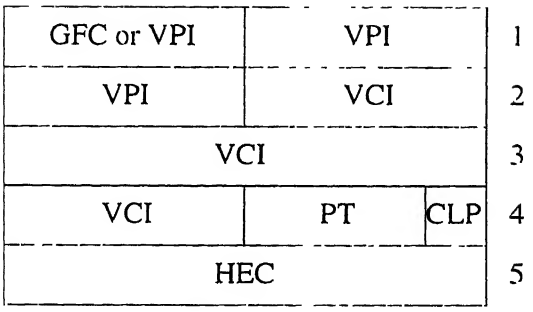


Figure 1.3 Header Structure

- Virtual Path Identifier (VPI) It tells the virtual path number for cell Virtual paths are used to switch the cell through high level cross connections [1] It is 8 bit field at User Network Interface and is increased to 12 bits at Network Network Interface (NNI)

- Virtual Channel Identifier (VCI) It provides the virtual channel number of the cell A virtual path connection carries a bundle of one or more virtual channels [2]

- Payload Type (PT) This 3 bit field is used to indicate the general type of data in the cell Typical uses of this field are to identify maintenance cells congestion conditions or the last cell of a multi-cell message

- Cell Loss Priority (CLP) It is a one bit field giving information about cell loss priority '0' represents high priority and '1' represents low priority Cells with low priority can be dropped in case of congestion

- Header Error Control (HEC) This 8 bit field provides a checksum over the cell header (but not including GFC if any) using CRC codes It can also correct one bit error HEC is also used to delineate the cells i e to identify the cell start and end in a synchronous stream

[1] See section 1.2.3
[2] See section 1.2.3

1.2.2 ATM User to User Communication Model

ATM connection between two users consists of the users at the end points and intermediate switching nodes (Figure 1.4) [2] In the connection two consecutive switching nodes are connected through physical link

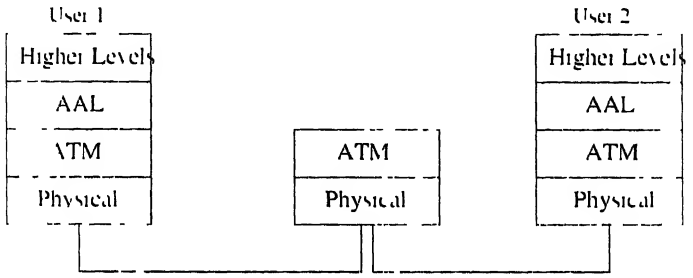


Figure 1.4 User to User Communication Model

1.2.2.1 Physical layer

The physical layer is subdivided into two sublayers namely Physical Medium (PM) and Transmission Convergence (TC) sublayers Then functions are as follows

PM sublayer does the following

- Bit transmission capability including bit alignment
- Electrical to optical and optical to electrical conversions
- Line coding decoding

TC sublayer does the following

- Cell delineation to recover cell boundaries
- HEC generation and checking
- Generation and recovery of transmission frames

- Transmission frame adoption

The physical layer receives cells from ATM layer transmits them on physical medium Similarly cell received from physical layer are sent to ATM layer

1.2.2.2 ATM Layer

ATM layer interfaces with physical layer and ATM Adaptation Layer (AAL) It interacts with physical layer through a physical service access point using the request and indicate primitives Interaction with AAL is through ATM service access point

ATM layer does the following

- Cell header generation and extraction
- Routing cells using VCI and VPI fields
- Cell multiplexing and demultiplexing
- Flow control at the User Network Interface (UNI).

1.2.2.3 ATM Adoption Layer (AAL)

This layer takes care of various kind of services to be offered by ATM network Since ATM network are supposed to provide various kind of services there are different kind of AALs for supporting each of these services

In order to define AAL requirements service classification has been made with respect to variable bit rates, connection modes and timing relationships Four classes of services A, B, C, D have been defined to support different types of traffic This classification and the corresponding AAL types are shown in Table 1 1

	Class A	Class B	Class C	Class D
Time Constraint	Required		Not required	
Bit Rate	Constant	Variable		
Connection Mode	Connection Oriented			Connectionless
AAL Type	AAL1	AAL2	AAL5	AAL3/4

Table 1.1 Classification of Services and AALs

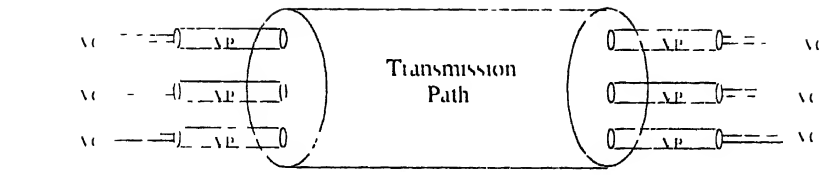
1.2.3 ATM virtual channels and paths

In ATM networks the connections are maintained by two identifier structures the virtual channel identifier and virtual path identifier They jointly identify each virtual circuit on a link A virtual channel is a concept used to describe unidirectional transport of ATM cells associated by a common unique identifier value' (CCITT I.113) This unique identifier is VCI which is valid in one direction A virtual Path is a concept used to describe unidirectional transport of cells belonging to virtual channels that are associated by a common identifier value' (CCITT I.113) This is VPI which is also valid in one direction [4]

Many virtual channels form a virtual path and many virtual paths form a transmission path (Figure 1.5) A set of VCI VPI value identify the complete connection between source and destination When cells are switched at node, the VCI and VPI values are translated to a new values The table of this mapping is maintained at each switching node by the network management function

1.2.4 ATM switching

As already mentioned an ATM switch changes the VCI VPI values of a cell header based upon routing table and routes it further by switching it to appropriate port At a switch either both VCI and VPI values or only VPI values are changed Correspondingly there are VC and VP switches which change both VCI VPI or only VPI respectively They are shown in



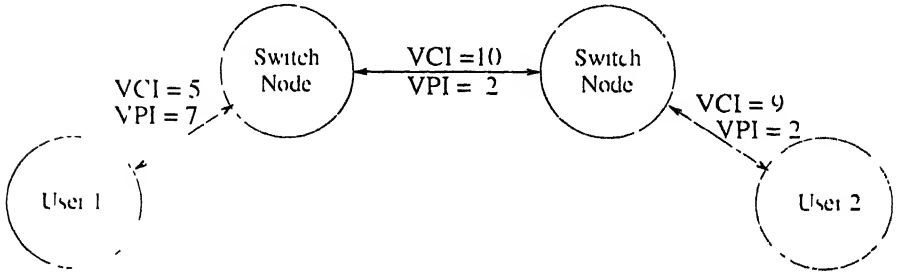


Figure 1.5 ATM Transmission

Figure 1.6 It is important to note that cells associated with a particular VCI VPI value in a cell header are transported along the same path so that cell sequence is preserved [4]

1.2.5 Header Replacement:

In ATM switch node a new header is generated with new VCI VPI, CLP values at ATM layer. This is used to replace the old header in the cell. Thereafter HEC is computed and placed in the header in physical layer. These function are performed before the actual switching process. Before the replacement of header the switching node starts keeping the track of cell till it is switched to output port. This makes the switching decision independent of new header.

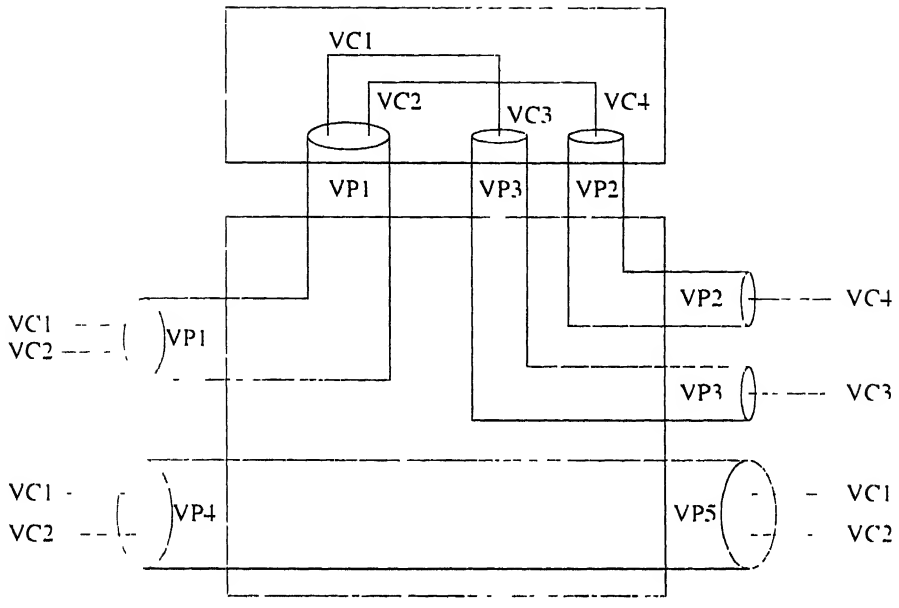


Figure 1.6 ATM Switch

1.3 Objective of the Thesis

In this work an effort has been made to investigate possibility of integration of optical header replacement mechanism and optical switching. For this purpose first information on optical header replacement has been collected. Then possibility of integration of different methods of optical header replacement with an optical switch has been considered. Finally for the new switch architecture computational noise analysis has been done.

1.4 Organisation of the Thesis

Chapter 2 tells various issues in switching. It also gives an overview of optical switching technologies. Chapter 3 discusses various techniques of optical header replacement. It proposes the design for integration of header replacement and switching. It further discusses its pros and cons. Chapter 4 gives

mathematical models of different components of loop It also give mathematical formulation of noise analysis for the loop Using computation result the performance of loop with header replacement mechanism is given in chapter 5 It is compared with the loop without header replacement mechanism

Chapter 2

Switching Technologies

At switching node the VCI VPI values are read from the header of incoming cell and outgoing link is determined by a lookup table using VCI VPI values The VCI VPI values are updated and cell is switched to the outgoing link At any switching node one or both identifier (VCI or VPI) are changed depending on whether it is a VC or VP switch The switching node also allocates the VC and VP numbers to any connection during connection set up These VCI VPI values are entered in routing table at the time of call set up and deleted at the time of call termination

Design of a switch is affected by various factors A few of these are given below [5]

- The bit rate of traffic that flows through the switch
- Congestion
- Decision of priority of cells during congestion
- Buffering

A simple model of a switching node is shown in Figure 2 1 It consists of a switching fabric protocol machine and I O interfaces. Switching fabric

does the switching of cells from incoming links to outgoing links It is up to a large extent a hardware structure The I O interface performs physical level preprocessing and header formation The complete control of switching fabric and I O interface is done by protocol machine It maintains complete routing table Depending upon the requirements the architecture of the switching fabric may be of three kind Shared Memory architecture, Shared Medium architecture and Space Devision architecture

Similarly the buffering in switching fabric may be of three kind Input Buffering Output Buffering and Intermediate Buffering Also modes of message transfer may be of three kind . Time Devision Multiple Access (TDMA) Wavelength Devision Multiple Access (WDMA) and Code Devision Multiple Access (CDMA)

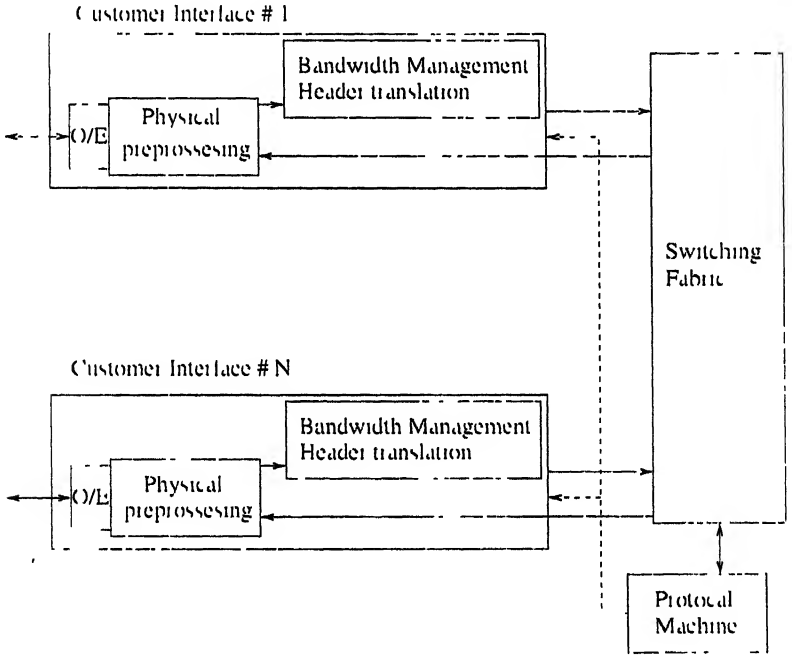


Figure 2 1 Switching Node

2.1 Architecture of Switching Fabric

2.1.1 Shared Memory Architecture

This architecture consists of a single dual port memory module shared by all input and output ports. Here the incoming cells are multiplexed into a single stream written into the memory, read out demultiplexed and transmitted to the output lines. The main drawback in this method is the memory access time to support the both incoming and outgoing cells.

The memory can logically be organised into full sharing mode or partitioning mode. In first case the entire memory is shared by all output and input ports and an arriving cell is dropped only when the memory is full. In the second case an upper bound is imposed on the number of cells waiting in the queue of each output port and a cell is dropped if this limit is reached in a particular queue even if there is space in the memory. Full sharing provides a better cell loss probability than the complete partitioning, because of more effective utilisation of memory. But this scheme is not fair at times when a burst of cells arrive at a particular output port, reducing the space available and eventually causing the service degradation for other ports. A typical shared memory switch is shown in Figure 2.2.

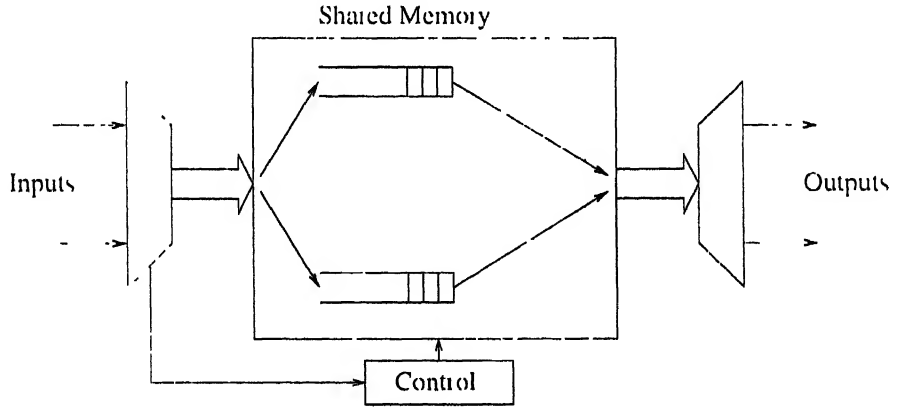


Figure 2.2 Shared Memory Switch

2.1.2 Shared Medium Architecture

In this architecture the incoming cells are multiplexed into a common medium typically a bus or a ring The medium speed is in general greater than or equal to the sum of transmission rates of incoming links Here a small FIFO (First in First Out) which has capacity to hold a few cells is used to store incoming cells until they access the medium In this architecture the output contention can not occur as two or more cells can not arrive at an output port simultaneously However the arrival rate of the cells may exceed the link capacity for a short period of time Hence output buffers are used to store these cells The disadvantage of this architecture is that as the number of links and then speed increases, the medium speed become a constraint Hence these switches can not be run at high speed So this architecture is mostly used in small work-group switches or as switching element of larger backbone switch A typical shared medium switch is shown in Figure 2 3

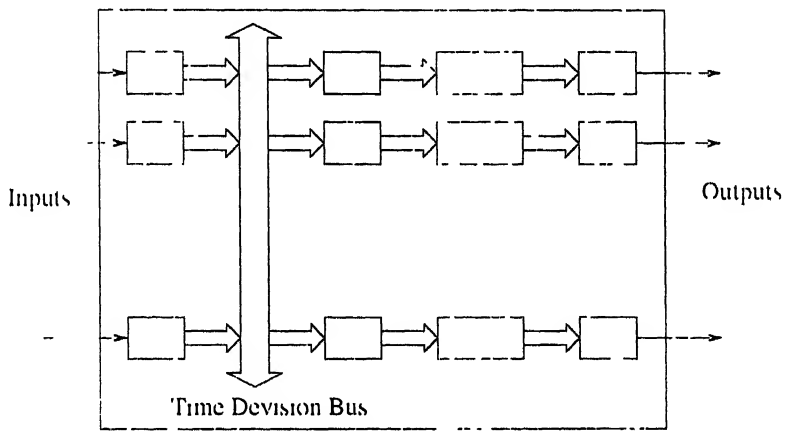


Figure 2 3 Shared Medium Switch

2.1.3 Space Devision Architectures

In these architectures the space devision cross bar switches are used as basic elements Here each cell transfer requires the establishment of a dedicated

physical path through the switch from incoming to outgoing links. Multiple cells from different inputs can be transferred concurrently on multiple links. These switches also allow the control to be distributed within the switch thereby reducing the complexity. Whole of the switch is implemented using a single large cross bar switching element or many small cross bar elements forming banyan network, batcher banyan network or buffered banyan network as the basic switching fabric. Figure 2.4 shows a typical space devision switch using a single cross bar switching element.

In space devision architecture both output contention and internal contention can occur. Output contention occurs when more than one cells arrive at an output port simultaneously. Internal contention occurs when some link becomes common to two paths. To solve this problem buffers are used. They may be placed within the cross point or at the input port. In case the switch is internally non-blocking, output buffering can be used to resolve the output contention. Here finite buffer don't solve the problem of output contention completely because buffers can become full leading to dropping of cells. Several schemes with finite buffer sizes have been suggested in which the problem of cell loss due to path contention is taken care of.

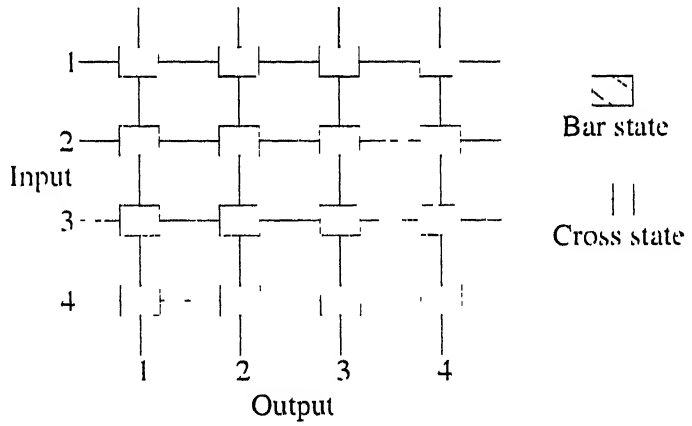


Figure 2.4 Space Devision Switch

2.2 Mode of Message Transfer

Several techniques have been developed for multiplexing many signals over a single physical channel to provide multiple access to user. There are three widely used multiple access techniques viz. TDMA, WDMA and CDMA [1]

2.2.1 Time Devision Multiple Access (TDMA)

In this scheme a single bit duration is broken up into small subintervals whose number is equal to that of connections to be multiplexed. Each connection uses a fraction of bit interval to send its own information bit. The scheme is shown in Figure 2.5

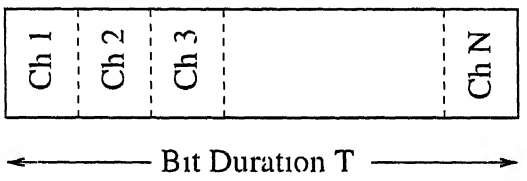


Figure 2.5 Time Devision Multiple Access Scheme

2.2.2 Wavelength Devision Multiple Access (WDMA)

In this scheme each connection is assigned different wavelength over which its signal is modulated and send simultaneously. At the receiving end the signals are separated by the tunable or fixed filters. Spectrum for WDMA system is shown in Figure 2.6

2.2.3 Code Devision Multiple Access (CDMA)

In this scheme data to be transmitted is encoded using codes. The code used are chosen to be orthogonal with each other. Each of the transmitters can be assigned different codes. The receiver can use a correlater to find out which transmitter is transmitting what. In order to maximise the performance of

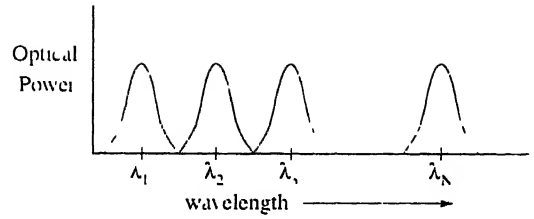


Figure 2.6 Wavelength Devision Multiple Access Scheme

code devision multiple access systems, the autocorrelation of all the codes should be a delta function and cross correlation between any two codes should be minimum (ideally zero)

2.3 Types of Buffering Schemes

The buffering is needed to resolve the contention. There are three major approaches to provide buffering. Input Buffering, Output Buffering and Intermediate Buffering. In all the three approaches the buffers can be shared or non-shared. The input buffered switch has the advantage that the switching speed required is the same as the number of inputs whereas it has disadvantage that the maximum available throughput is 0.586 due to the head of line blocking phenomenon [2]. Output buffer switch has a throughput of 1.0 but but the switching speed required is of the order of the square of number of inputs [2]. Intermediate buffering tries to take the best of both but as a result is more complex. So it is rarely used.

In the case of non-shared buffer scheme the advantage is that the control logic is simple and the backplane interface switching speed are the least. but a serious disadvantage of this scheme is that the effective buffer utilisation is grossly reduced and as a result the cell loss probability per unit buffer size increases. The advantage of shared buffer scheme is that the effective utilisation of buffer is maximum and as a result the cell loss probability per unit buffer size is less. but a serious disadvantage is that the control logic

becomes more complex and the backplane switching speed becomes N time the link data rate for a $N \times N$ switch [2]

2.4 Survey of Optical Switches

The efforts for development of optical switches are going on since the last decade The requirement for an optical switch will be system dependent but the following features are desirable in all-optical switches [6]

- Polarisation Independent
- Low crosstalk
- Low insertion loss and even gain
- Wavelength independence
- Multi-wavelength operations
- Bit rate transparency
- Fast switching
- Simple implementation
- Scalability

The continuous efforts have resulted in some general approaches for realisation of optical switches Few of these general approaches are described here Some of these are suitable for circuit switches and some for packet switches

2.4.1 Directional Coupler

It consists of two coupled waveguides (Figure 2.7). They are characterised by their coupling length and the bias voltage or current to achieve a π phase shift in interferometer. They require only small index change and can therefore be fabricated either with electro-optic carrier depletion or carrier injection waveguide. Many directional couplers are combined to make a large switch. Directional coupler based monolithically integrated large switches have also been made. The biggest drawback of these switches is that they are polarisation sensitive due to different coupling length for TE and TM modes and polarisation sensitive electro-optic effect. The other drawback is that the control of coupling length is difficult during manufacturing. The limitation of polarisation sensitiveness can be overcome, even though it is difficult [6].

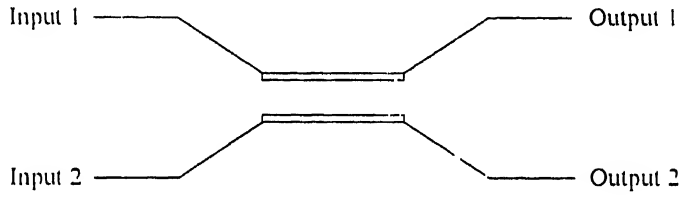


Figure 2.7: Schematic View of a Directional Coupler

2.4.2 Mach-Zehender Interferometer Switches

For realising Mach-Zehender interferometric switch, the 2×1 Y-junction of Mach-Zehender interferometer are replaced by 2×2 mode couplers as shown in Figure 2.8.

An important advantage of Mach-Zehender interferometric switch as compared to the directional coupler is the geometrical separation of mode coupling and phase shifting regions. Thus here independent optimisation is possible and switch can be easily made polarisation insensitive. MZI switches are well suited for high speed applications. In addition to 2×2 MZI switches, $N \times N$ MZI switches have also been realised demonstrating polarisation

insensitive switching. Here for polarisation insensitiveness the multi mode Interface (MMI) couplers are used [6]

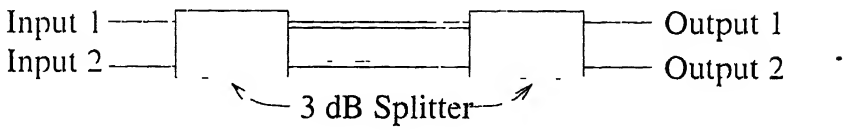


Figure 2.8 Integrated Optical Mach-Zehender Interferometer Space Switch

2.4.3 Digital Optical Switches

The digital optical switch (DOS) (shown in Figure 2.9) is based on adiabatic mode evolution in contrast to directional couplers and Mach-Zehender interferometers that use interference effects [6]. Consequently polarisation insensitive operation can be obtained for DOS and it has large optical bandwidth in both TE and TM polarisation. It has digital response. The switching of DOS can be obtained by reverse or forward bias operations in the p-i-n heterostructure. Due to Y shape of junction the DOS acts as a 3 dB splitter when no bias is applied and easily provides broadcasting function which is needed in many system applications. Many Digital Optical Switches can be combined to make a large switch. For example a 4×4 switching matrix have been reported in a strictly non-blocking tree architecture with 24 DOS [6].

2.4.4 Active Space Switches

Here the gain modulators e.g. Semiconductor Optical Amplifiers (SOAs) are used for space switching applications. Most often the tree structure is used. An example is given in Figure 2.10. Here a fully connected shuffle network between input and output port is realised using adequate power splitters and combiners. Each connecting path can be switched on or off using the corresponding SOA. Therefore N^2 SOAs are required. Such a switching matrix inherently generates the splitting losses that can be important for large

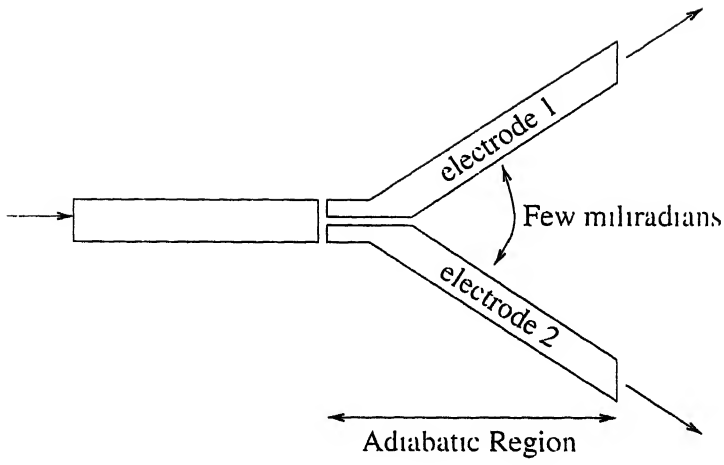


Figure 2.9 Schematic View of a Digital Optical Switch

switch arrays. To compensate for the losses, additional booster amplifiers can be included with the drawback of noise accumulation [6].

2.4.5 Switch based on Fiber Delay Lines

This switch relies on dynamic wavelength encoding and multiplexing for fast switching of cells [7]. The scheme is shown in Figure 2.11. Here the n-input n-output switching matrix consists of four functional block:

1. The cell encoder block, incorporating n fast tunable optical wavelength converters which assign wavelength to each cell corresponding to its target output.

2. The time-switching and buffering block consisting of mn fast optical gates which are used by each of the wavelength converter to access all the m wavelength devision multiplexed operated fiber delay lines. These fiber delay line have increasing lengths from $0 \times T$ to $(m-1) \times T$ where T is the cell period.

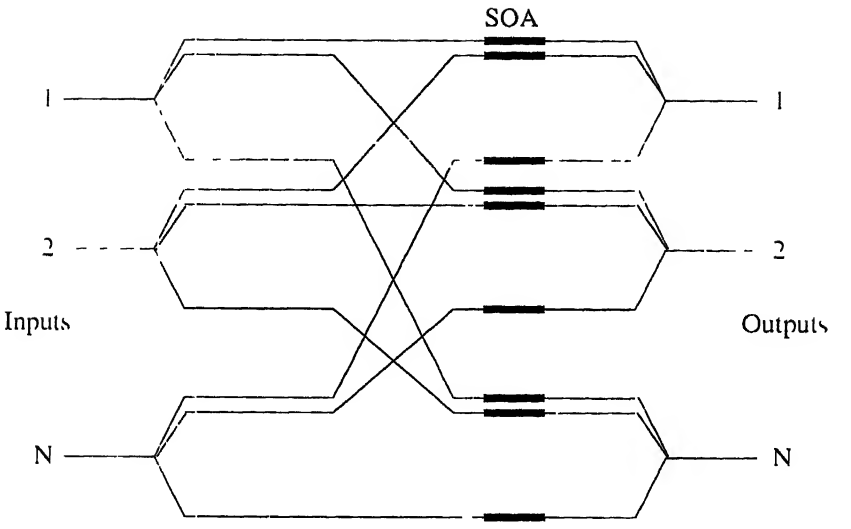


Figure 2.10 SOA based $N \times N$ Space Switch in a Tree Arrangement

3 The wavelength demultiplexer block including n bandpass filters, each tuned to a different wavelength, thus defining the output address

4 The electronic control block implementing the switching algorithm

In this architecture in any slot upto m cells can be directed to a output If more than m inputs contend for a output then some of the cells will be dropped

2.4.6 Switch Based on Fiber Optical Loop Memory

Recently an optical switch based on fiber optical loop memory (FOLM) has been proposed [13] In this thesis WDM version of this switch architecture has been considered The schematic is shown in Figure 2.12 The functioning of switch is as follows

The Tunable Wavelength Converter (TWC) modulates the incoming packets into an available wavelength The available wavelength is decided by the controller and it accordingly adjusts the TWC. All inputs are combined by star coupler

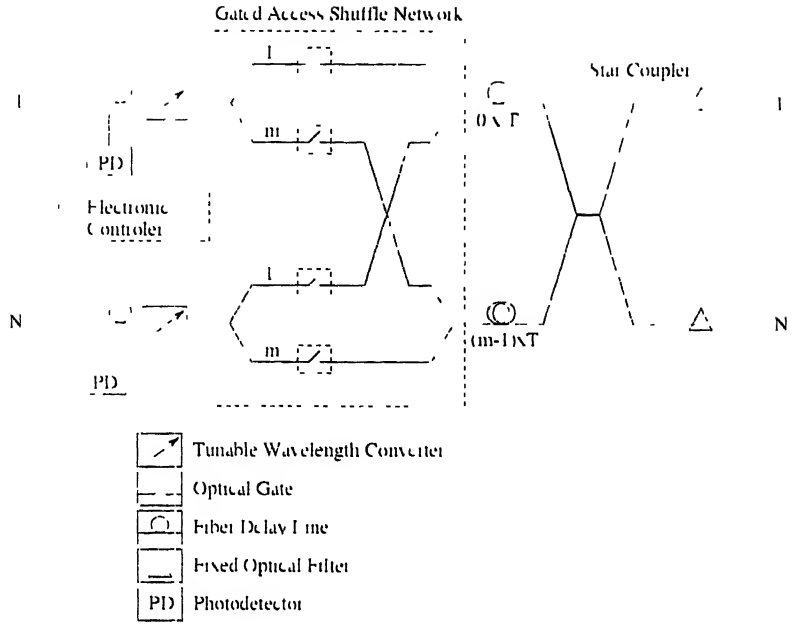


Figure 2.11 Delay Line Switching Matrix

In normal circumstances the packet is directly sent to output without storing it in FOLM. But sometimes when contention occurs i.e. two or more than two cells opt for same output, only one of these is sent to output and others are modulated into different wavelengths and are stored in the FOLM. They are sent to output port in next time slots. In case all wavelengths in fiber loop are in use, the cell is dropped. Thus fiber loop is used for contention resolution by WDM.

The fiber loop is made up of 3 dB coupler, WDM demultiplexer, Semiconductor Optical Amplifiers (SOA), WDM multiplexer and Erbium Doped Fiber Amplifier (EDFA). Due to 3 dB coupler the packets which are input to loop are visible to loop as well as to star coupler at output. Similarly the packet which completes rotations in the loop is also visible to loop as well as to star coupler at output. SOAs are used as optical gates and amplifiers. When some particular packet is passed out of switch by activating appropriate Tunable Filter (TF), the corresponding SOA is turned off in the same

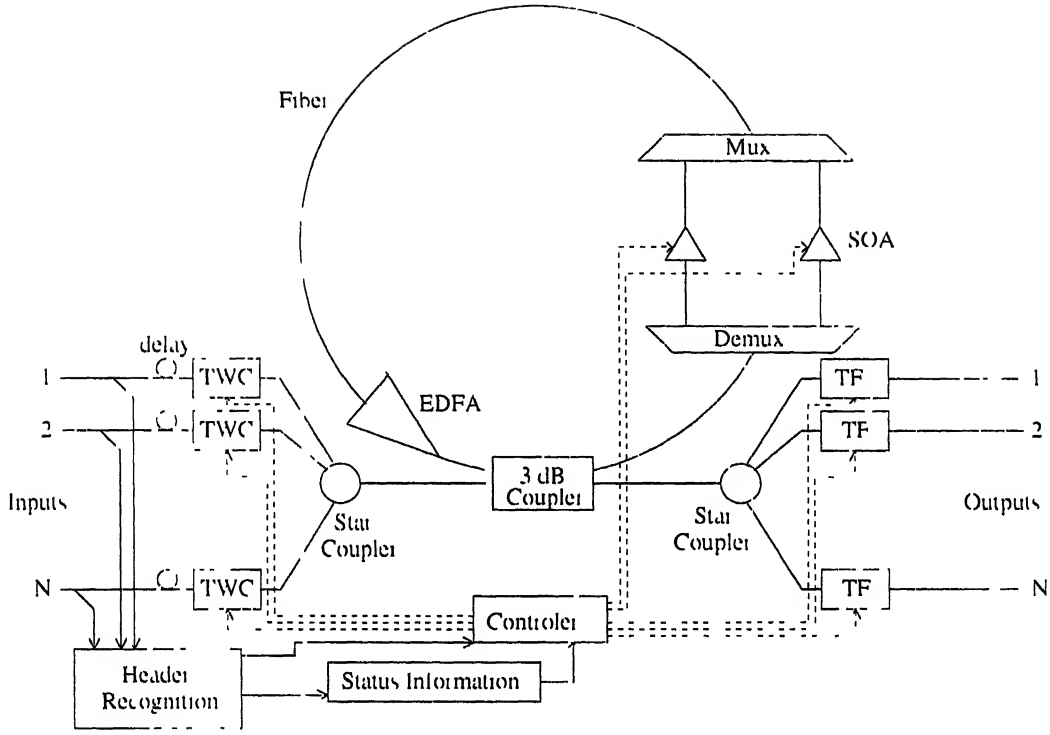


Figure 2.12 Optical Switch based on FOLM

time slot and thus wiping out packet from loop The EDFA also compensates different losses for example splitting loss

2.4.7 Multidimensional Switch

It aims at exploiting the wavelength domain for contention resolution to minimise the amount of optical buffer required in a multistage switching network arrangement Its basic matrix is shown in Figure 2 13 [7] In case of contention the cells competing at the same time for the same output of a switching element are converted to m free additional wavelengths and transmitted at the same time slot instead of being delayed in a buffer and then transmitted consequently This is achieved by activating appropriately the additional optical wavelength converters on each inlet Consequently the number of internal wavelengths of a switching elements must be extended being the price to pay for avoiding the use of the time domain

2.4.8 Ultrafast Photonic ATM Switch based on Bit-interleave Multiplexing

This switch is an upgradation of a switch based on cell-interleave multiplexing It is based on broadcast and select network and hence can handle multicast switching [8] Its block diagram is shown in Figure 2 14

Here the Input Module (IM) has a buffer and output contention resolution mechanism Optical Bit-Interleave Multiplexing module does bit interleaving with the help of ultra-short pulses of Short Pulse Laser Diode (SPLD) and intensity modulator (M) Optical Cell Selection Module selects desired cells on a slot-by-slot basis

In this Chapter we surveyed many switching techniques In the next Chapter we will be looking at the techniques for replacement of header in optical switches

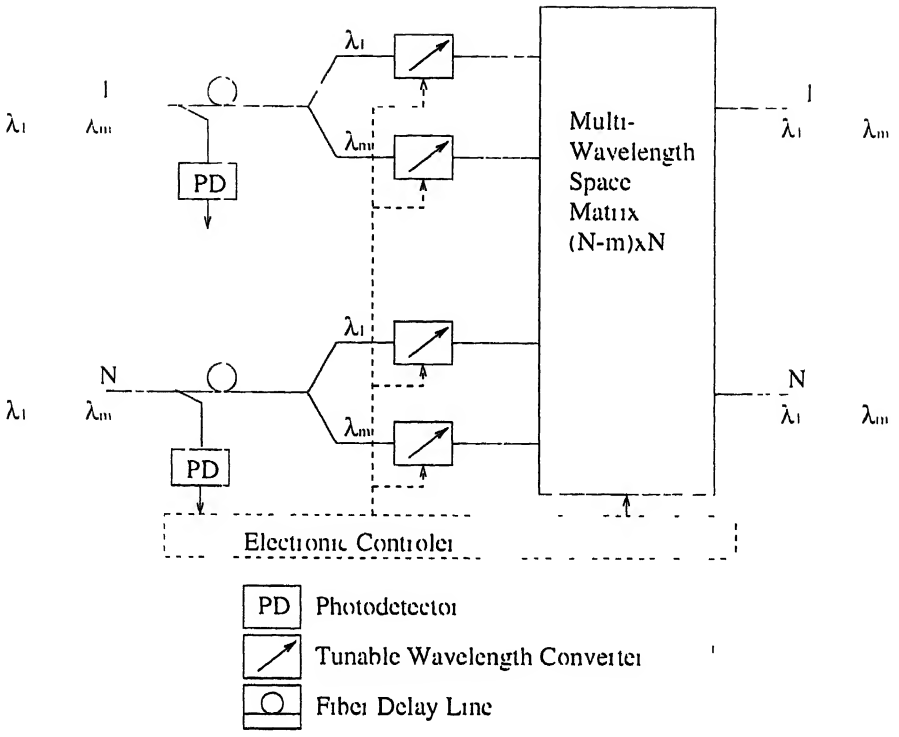
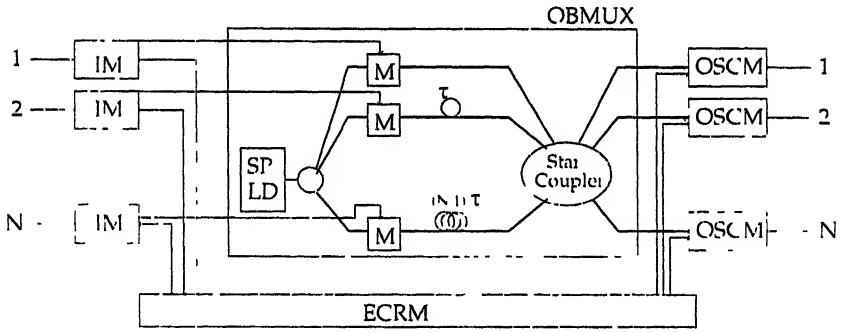


Figure 2.13 The Multidimensional Switching Matrix



IM Input Module
SPLD Short Pulse Laser Diode
OBMUX Optical Bit-Interleave Multiplexing Module
OCSM optical cell Selection Module
M Intensity Modulator
ECRM Electronic Contention Resolution Module

Figure 2.14 Block Diagram of Photonic ATM Switch Architecture

Chapter 3

Header Replacement in Optical Switching

3.1 Introduction

At present the header replacement in optical switches is carried out electronically. In this method first the optical header is converted into electronic form, then it is changed and again converted back into optical form.

Recently few attempts have been made for all-optical header replacement i.e. header is regenerated and replaced without converting into electronic form. Some of these methods are described in this Chapter.

3.2 Optical Header Replacement

3.2.1 Method I : Header Replacement using Continuous Wave

In this method [9] the cell format used is shown in Figure 3.1. It consists of original header (OH), a time gap called guard band (G1), continuous wave (CW) period and the payload. The guard band G1 separates the CW period

from the header to provide sufficient time for header to be processed by controller

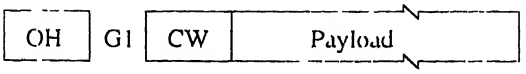


Figure 3.1 Cell Structure for Header Replacement in Method I

Here the scheme used for the header replacement is shown in Figure 3.2 An electronic controller monitors the input through a 10 dB splitter and an optical to electrical (O/E) converter. A fiber delay (alignment delay) is used to set timing in the output packet. Each of two SOAs, SOA1 and SOA2 receives an entire copy of input packet via 3 dB fiber splitter. Function of SOA2 is to modulate data onto the CW period to produce new header. SOA1 removes original header. The output of both SOAs are recombined by a 3 dB fiber coupler to produce output packet.

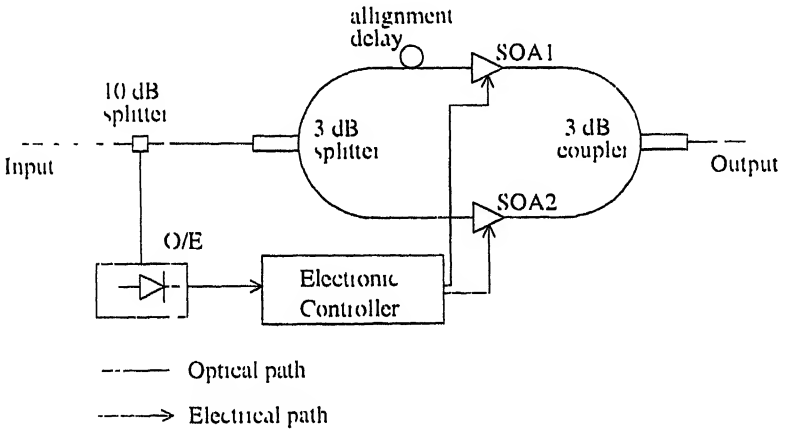


Figure 3.2 Scheme of Experimental Header Replacement in Method I

Figure 3.3 shows the timing diagram for header replacement. The electronic controller detects packets and accordingly controls SOA1 and SOA2. After CW period is detected, the controller starts gating SOA2 with new header information thereby modulating the light in the CW period. After

this controller turns off SOA2. SOA1 is turned on when guard is detected on SOA1 and turned off after payload.

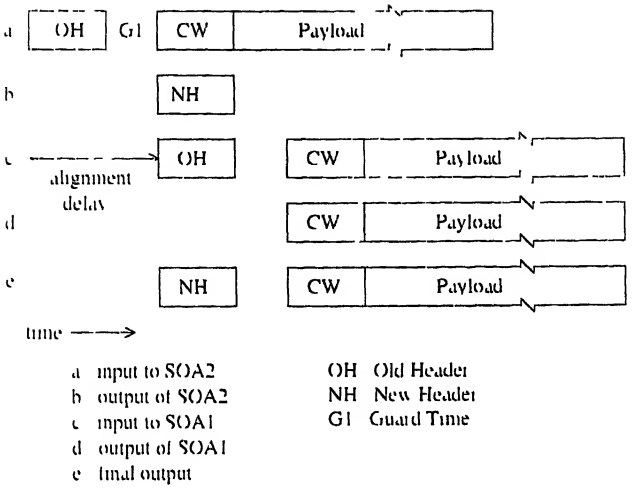


Figure 3.3 Timing Diagram for Header Replacement in Method I

3.2.2 Method II : Simultaneous All-Optical Packet Header Replacement and Wavelength Shifting

In this method [10], the wavelength shifting and header replacement is realised simultaneously using three level modulation of a probe laser. Here probe laser changes the header bits one-by-one effectively. The scheme for this is shown in Figure 3.4. It illustrates an incoming packet on λ_{pump} and its header being replaced simultaneously. When the entire header or an individual bit requires no change, wavelength shifting is performed by setting the probe input power to a middle level. When an individual bit requires change the probe input power is either decreased to a 'low' level , forcing a low probe output power or increased to a 'high' level, forcing a high probe output power. Here one should be careful for the fact that wavelength shifting using cross gain compression inverts the input bits.

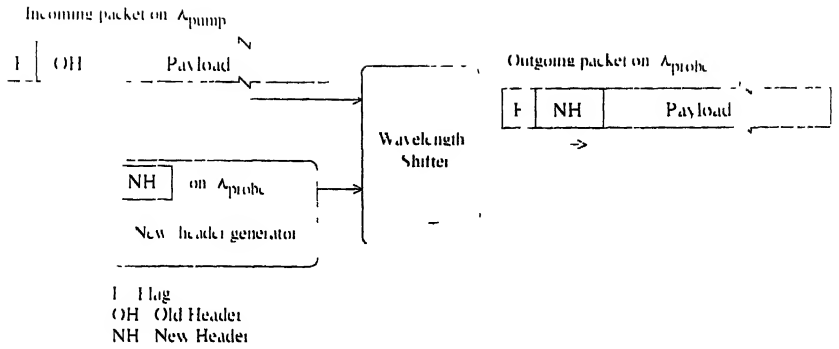


Figure 3.4 Scheme for Simultaneous Header Replacement and Wavelength Shifting

3.2.3 Method III : All-Optical Updating of Sub-carrier Encoded Packet Headers with Simultaneous Wavelength Conversion of Baseband Payload

The block diagram of this process is shown in Figure 3.5 [11] Here first of all simultaneous sub-carrier modulated (SCM) header suppression and wavelength conversion of baseband payload is achieved due to low pass frequency response of the cross gain modulation in a semiconductor optical amplifier and then the header replacement is performed by optically remodulating the wavelength converted signal with a new header at the original sub-carrier frequency

3.2.4 Method IV : Header Replacement using a Long CW Region Generated Directly from the Packet Flag

In this method [12] continuous wave (CW) is generated from packet flag It insures that there is no difference in wavelengths of new header and input packet The continuous wave from flag is generated by fiber loop Once CW is created it is optically modulated with new header which is added to

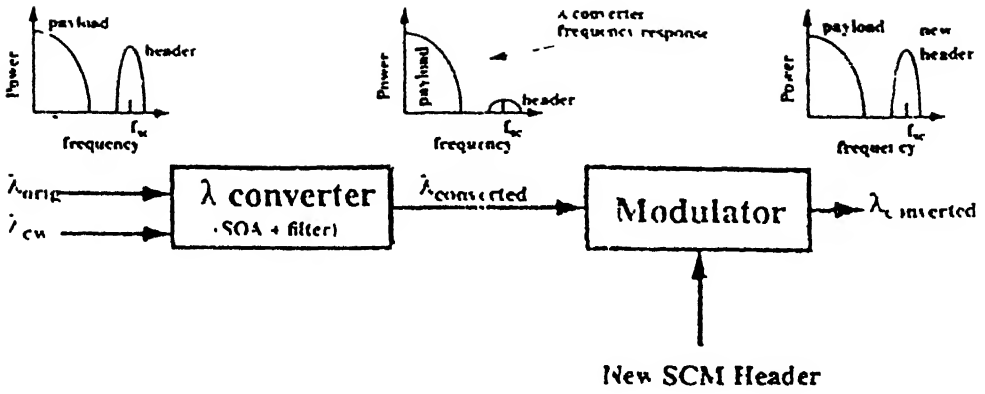


Figure 3.5: Updating of Subcarrier Encoded Packet Header with Wavelength Conversion of Payload.

payload of original packet. The schematic for this method is given in Figure 3.6.

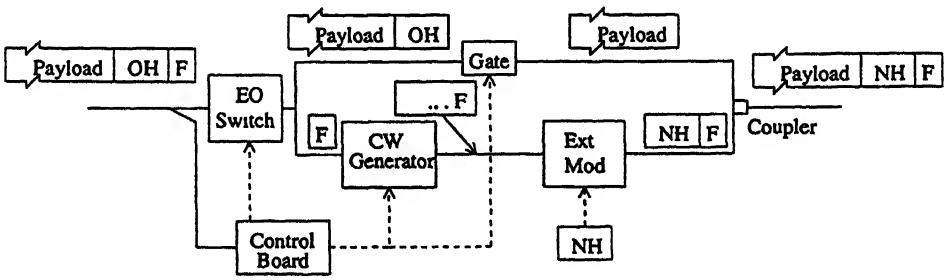


Figure 3.6: Schematic for Header Replacement using CW Region Generated from Flag

3.3 Proposed Integration of Header Replacement and Switching

As an innovative approach the integration of header replacement and switching has been proposed here. For this purpose the method of header replace-

ment (described in Section 3.2.1) and the optical switch described in Section 2.4.6 have been used. The integrated scheme is shown in Figure 3.7

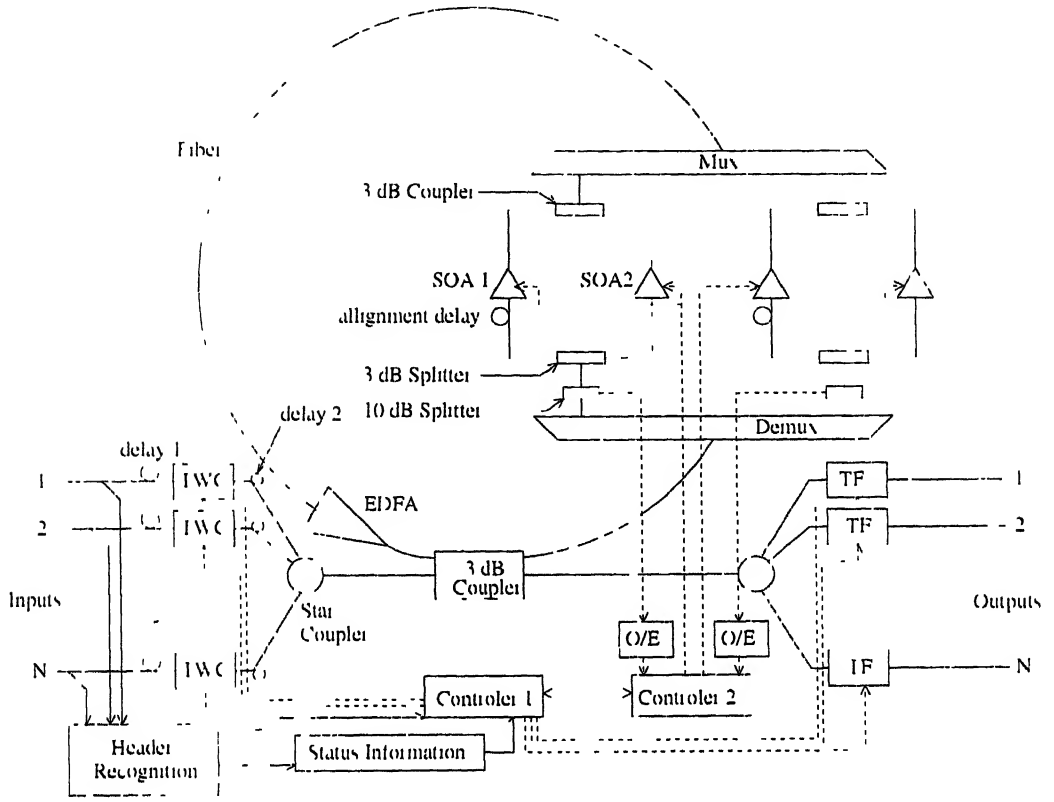


Figure 3.7 Model for integration of Header Replacement and Switching

The above scheme not only proposes a new concept of combining header replacement and switching but it also gives economical advantage in terms of saving of an SOA for each channel in comparison to situation where header replacement is separated from switching. At the same time the cost in terms of control complexity increases. Obviously there is one limitation that every packet would have to make at least one rotation in the loop while passing through the switch (for header replacement to be carried out).

Here one should note that integration of method III described in Section 3.2.3 with switch described in Section 3.3 is not possible because Suppressed

Carrier Modulation (SCM) scheme is not being used in the switch. Similarly method II of header replacement can not be integrated because it does the wavelength shifting simultaneously. Also many laser sources would be needed which will always remain ON and hence would lead to serious loss of power. The method IV of header replacement does not have these objections but its use in the switch will make the switch very complex due to presence of CW generator in the header replacement mechanism which is realised through fiber loops.

Following are the main feature of the proposed architecture.

1. The cell can be sent to an output only after header replacement is done. Hence there is no gain in terms of time saving. Also since header replacement is done in each cell, it will have to make at least one rotation in the loop.

2. We need to add delay (Delay 2 in Figure 3.7) just after Tunable Wavelength Converter (TWC) for the time required to compute new header.

3. In this architecture, significant power is lost in the mechanism for header replacement, which leads to larger gain via SOA and EDFA in general. Hence Amplified Spontaneous Emission (ASE) noise from SOA and EDFA are more and thus noise in one rotation of cell is larger in comparison to the situation when header replacement mechanism is not used. Thus allowed number of rotations in loop would be less.

4. The sum of alignment delay and time taken in the loop should be equal to the length of the packet. Since the alignment delay is equal to the time of old header plus guard ring (see Figure 3.3), the length of loop should be equal to length of 53 bytes (assuming the length of CW period is equal to that of header).

3.4 Issues in the Proposed Architecture

There are three main issue in the proposed architecture

- Noise Analysis
- Timing Analysis
- Electronic Control Mechanism

In the present work, the noise analysis of proposed architecture i e loop with header replacement mechanism is done and compared with loop without header replacement mechanism

Chapter 4

Computational Model of Loop

4.1 Model for Coupler and Splitter

A coupler or splitter can be considered as four port device as shown in Figure 4.1 [14]. Two of these ports are input ports and two output ports. Let port 1 and 2 are input ports through which power P_1 and P_2 is send in the device respectively. Let port 3 and 4 are the output ports through which power P_3 and P_4 is obtained.

Assume $P_2 = 0$ then splitting loss (α) for port 1 is defined as

$$\alpha = 10 \log_{10} \frac{P_4}{P_3 + P_4} \; dB \tag{4.1}$$

Some of the optical power is lost while going from input to output ports. This loss is termed as excess loss and is given by

$$excess\ loss \;=\; 10 \log_{10} \frac{P_4}{P_3 + P_4} \; dB$$

Insertion loss is defined as sum of excess loss and splitting loss

$$Insertion\ loss \;=\; |splitting\ loss| + excess\ loss$$

$$insertion\ loss\ =\ 10\log_{10}\frac{P_1}{P_4}\ dB$$

Figure 4.1 Coupler and Splitter as Four Port Device

In the same way as above the splitting loss, excess loss and insertion loss for port 2 can be defined. For a 3 dB coupler they are assumed to be same for the both ports. Mostly the excess loss for couplers and splitters is 0.5 dB.

4.2 Model for Multiplexer and Demultiplexer

4.2.1 Multiplexer

Multiplexer is realised by connecting 2×2 couplers in succession. For example a multiplexer for 8 inputs can be realised in the manner shown in Figure 4.2. Here each box represents 3 dB coupler.

It is obvious that if number of channels (inputs) is more than 4 and less than or equal to 8 then 3 stages of couplers will have to be used. Hence we can say that if number of channels is M then multiplexer loss for each channel is

$$Loss_{mux} = \lceil \log_2 M \rceil\ 3$$

where $\lceil r \rceil$ represents the integer just greater than r and 3 represents insertion loss for a coupler. If excess loss for a 3 dB coupler is taken as 0.5 dB then

$\beta = 3.5 dB$

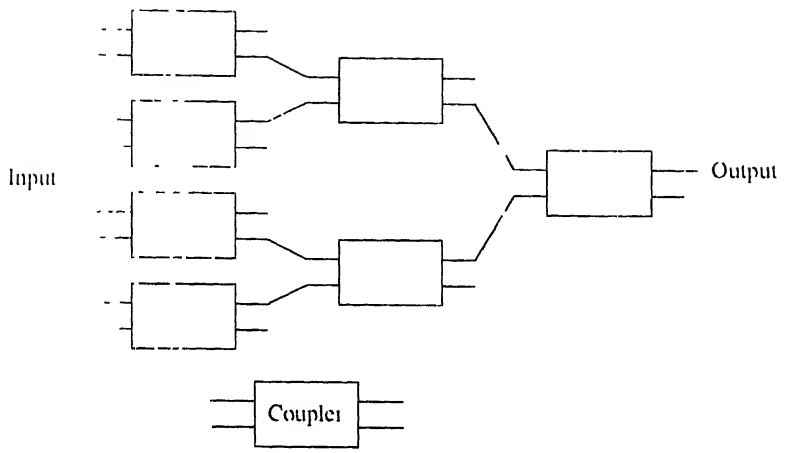


Figure 4.2 WDM Multiplexer

4.2.2 Demultiplexer

Demultiplexer is also realised by connecting 2×2 couplers in succession and using filters after them. For example $1 - 8$ demultiplexer is realised in the manner shown in Figure 4.3.

Here too, if number of channels (output) is more than 4 and less than or equal to 8 then 3 stages of couplers will be used. Thus if number of channels is M then demultiplexer loss for each channel is :

$$Loss_{demux} = \lceil \log_2 M \rceil \beta + L_f$$

where $\beta = 3.5\ dB$ for 3 dB coupler and L_f is filter loss.

It is assumed that filters are ideal. Hence $L_f = 0$ and crosstalk due to filter is zero.

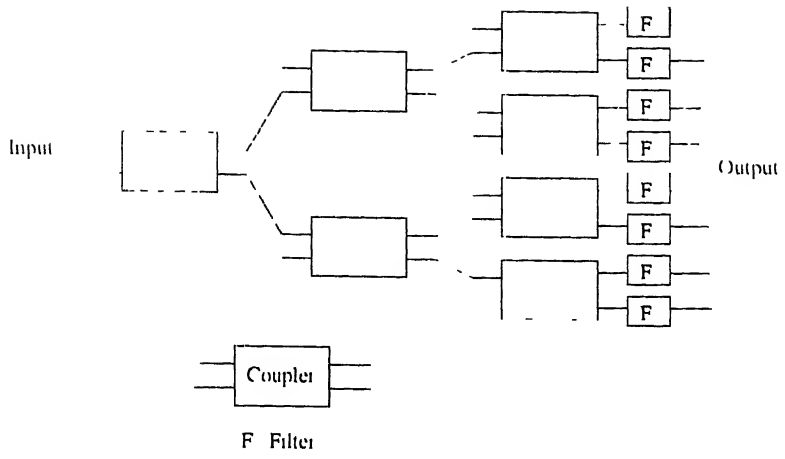


Figure 4.3 WDM Demultiplexer

4.3 Model for Semiconductor Optical Amplifiers

The SOA is basically semiconductor laser which operate below lasing threshold. Electrical energy is used to achieve the population inversion in these. The basic difference between a laser and SOA is facets reflectivity. Ideally SOA should have zero reflectivity and for a laser it should be one for a facet and less than one for other facet. SOA which has very low reflectivity is called traveling wave amplifier (TWA) since input signal passes through device gain region only once. If facet reflectivity is reasonable but still quite small then signal passes back and forth through the cavity gain region many times and the device is called Fabry Perot Amplifier (FPA) [15]

4.3.1 Gain

A Traveling wave amplifier has anti-reflection coating applied to its facets to reduce their reflectivity. In the limiting case, an amplifier with zero reflectivity facets would be a traveling wave amplifier, with factor $G\sqrt{R_1 R_2}$ equal to zero, where G is the single pass gain through the device and R_1 and R_2

are the input and output facets reflectivity of the amplifier respectively In practice however even with the best anti-reflection coating there is some residual facet reflectivity and the amplifier lies between traveling wave amplifier and fabry-perot amplifier So an amplifier is defined to be traveling wave amplifier if $G\sqrt{R_1 R_2} \leq 0.17$ For a TWA the gain is given by [15]

$$G = G_0 \exp\left(-(G-1)\frac{P_{in}}{P_{sat}}\right)$$

where

$$\begin{aligned} G_0 &= \textit{Unsaturated gain} \\ P_{in} &= \textit{Input power level} \\ P_{sat} &= \textit{Saturation power level} \\ G &= \textit{Gain} \end{aligned}$$

G_0 and P_{sat} depend on amplifier and biasing condition This equation is derived from steady state analysis and ignores dynamic effects [15]

The contrast ratio for a Semiconductor Optical Amplifier is defined by

$$\textit{Contrast Ratio} \quad R_c = \frac{G_0}{G_{off}}$$

where G_{off} is the gain when SOA remains off Contrast ratio is a finite number Hence G_{off} is not exactly zero Thus when SOA remains off a small amount of signal is also passed through it which is called crosstalk and is treated as noise

4.3.2 Noise

In semiconductor optical amplifier when input signal is amplified, the spontaneous emission also occurs This spontaneous emission gets amplified and

is termed as Amplified Spontaneous Emission (ASE) noise. It is modeled as white Gaussian noise with power spectral density

$$S_{sp} = n_{sp}(G-1)h\nu \quad watts/Hz$$

So noise power is given by $N_{sp} = n_{sp}(G-1)h\nu\Delta B$ *watts*
where

$$\begin{aligned} n_{sp} &= \textit{Spontaneous emission factor} \\ G &= \textit{Amplifier gain} \\ h &= \textit{Planck constant} \\ \nu &= \textit{Frequency of input signal} \\ \Delta B &= \textit{Optical Bandwidth} \end{aligned}$$

4.4 Model for Erbium Doped Fiber Amplifier

It is made by doping the core of fiber by erbium (a rare earth element). The basic principal of EDFA is also based on the stimulated emission like SOA but optical pumping is used in place of electrical pumping for population inversion. Pumping power can be injected in three ways. It may be injected so that it may propagate in the same direction as the signal. Alternatively it may be injected in the opposite direction of signal. The fiber may be pumped by injecting pump power in forward as well as reverse direction for high output power amplifier. The signal amplification depends upon the population inversion profile along the fiber and also on the length of the fiber. For optimum gain we will have to trade off between pump power and length of fiber [15]

4.4.1 Gain

In Erbium Doped Fiber Amplifier (EDFA) the optical amplification is achieved by the process of stimulated emission as in SOA. For the stimulated emission the population inversion is required in the lasing medium. EDFA operates as three level system at room temperature. It can be modeled as shown in Figure 4.4

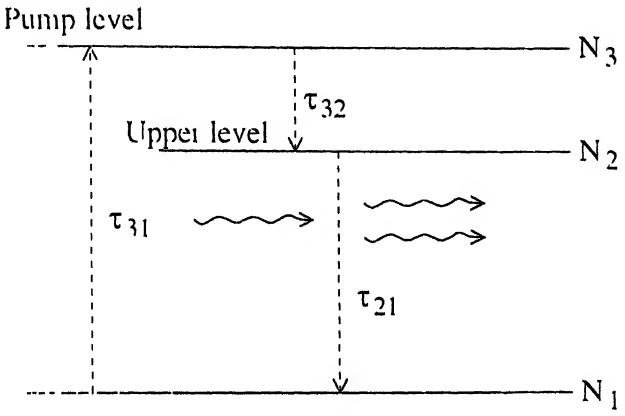


Figure 4.4 Three Level Amplification

From Figure 4.4 one can write [16]

$$\frac{dN_1}{dt} = -\frac{\sigma_p I_p}{h\nu_p} N_1 + \frac{N_2}{\tau_{21}} + (\sigma_e N_2 - \sigma_a N_1)\frac{I_s}{h\nu_s}$$
$$\frac{dN_2}{dt} = \frac{N_3}{\tau_{32}} - \frac{N_2}{\tau_{21}} - (\sigma_e N_2 - \sigma_a N_1)\frac{I_s}{h\nu_s}$$
$$\frac{dN_3}{dt} = \frac{\sigma_p I_p}{h\nu_p} N_1 - \frac{N_3}{\tau_{32}}$$

where

N_1 = *Ground level density*

N_2 = *Excited level density*

N_3 = *Upper level density*

σ_p = *Absorption cross section at* ν_p

σ_e = *Stimulated emission cross section at* ν_s

σ_a = *Absorption cross section at* ν_s

ν_p = *Pump frequency*

ν_s = *Signal frequency*

I_p = *Pump beam intensity*

I_s = *Signal beam intensity*

τ_{31} = *Level 1 to level 3 decay time*

τ_{32} = *Level 3 to level 2 decay time*

τ_{21} = *Level 2 to level 1 decay time*

h = *Planck constant*

Further rate equations for pump power $P_p(z, \nu_p)$ and the signal power $P_s(z, \nu_s)$ long z axis are given by [17]

$$\frac{dP_p(z,\nu_p)}{dz} = -\gamma_p(z, \nu_p) P_p(z,\nu_p) \tag{4.2}$$

$$\frac{dP_s(z, \nu_s)}{dz} = (\gamma_e(z,\nu_s) - \gamma_a(z, \nu_s)) P_s(z, \nu_s) \tag{4.3}$$

where

γ_p = *Absorption coeff for pump power*

γ_a = *Absorption coeff for signal power*

γ_e = *Emission coeff for signal power*

Now for uniform pump distribution and constant erbium concentration profile and where signal mode profile depends only on radius, it can be shown

$$\gamma_p(z,\nu_p) = \frac{\rho_0\sigma_p(\nu_p)}{\frac{P_p(z)}{P_p^{th}}+1} \tag{4.4}$$

$$\gamma_e(z,\nu_s) = \rho_0\sigma_e(\nu_s)(1-\eta)\frac{P_p(z)/P_p^{th}}{\frac{P_p(z)}{P_p^{th}}+1} \tag{4.5}$$

$$\gamma_a(z,\nu_s) = \rho_0\sigma_a(\nu_s)(1-\eta)\frac{1}{\frac{P_p(z)}{P_p^{th}}+1} \tag{4.6}$$

where

$$\begin{aligned} \rho_0 &= \textit{Erbium concentration} \\ P_p^{th} &= \textit{Threshold pump power} \\ \eta &= \textit{Overlap factor} \end{aligned}$$

such that

$$P_p^{th} = \pi R_0^2 \frac{h\nu_p}{\sigma_p \tau}$$

and

$$\eta = exp\left(-\frac{R_0^2}{\omega_s^2}\right)$$

where R_0 is fiber core radius, ω_s is the power spot size of the signal mode and $\tau = \tau_{21}$

Thus by substituting value of $\gamma_p(z,\nu_p)$, $\gamma_e(z,\nu_s)$ and $\gamma_a(z,\nu_s)$ from equation 4.4, 4.5 and 4.6 into equations 4.2 and 4.3 we get two dependent differential equation for $P_p(z,\nu_p)$ and $P_s(z,\nu_s)$ which can be solved by numerical method[1] to find value of $P_p(z,\nu_p)$ and $P_s(z,\nu_s)$ at given value of z

[1] The numerical method used is Runga Kutta fourth order method [19]

An important issue in above model is the absorption and emission cross section at different wavelengths. As such there is no formula for them. They are found experimentally. An experimental cross section around $\lambda = 1.531\ \mu m$ is shown in Figure 4.5.

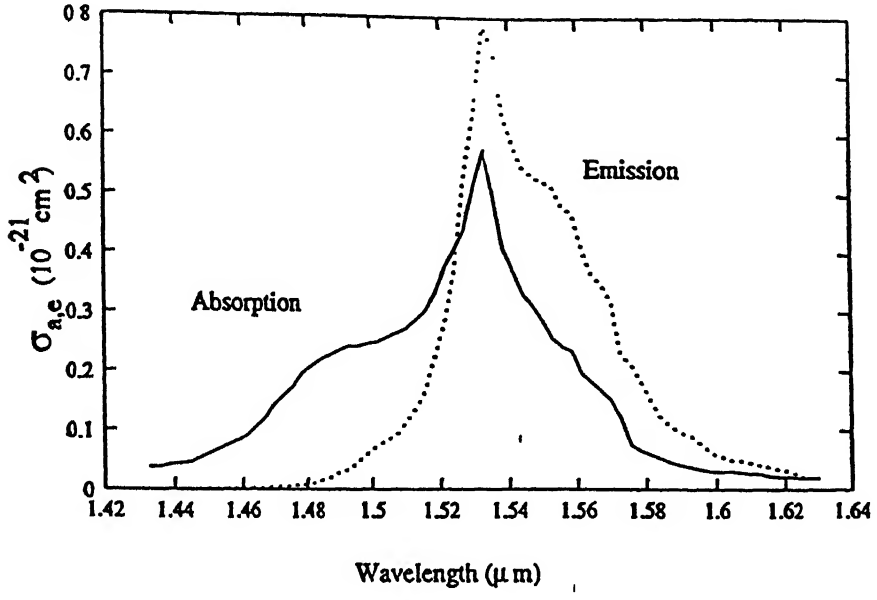


Figure 4.5: Experimental Cross Section around Wavelength $\lambda = 1.531\ \mu m$

An engineering approximation to above can be made as following [17]:

$$\sigma_a = \begin{cases} 4.83exp\left(-\frac{(\lambda-1.531)^2}{0.003}\right), & 1.4 < \lambda \leq 1.531 \\ 4.83exp\left(-\frac{(\lambda-1.531)^2}{0.00078}\right), & 1.531 < \lambda < 1.6 \end{cases}$$

$$\sigma_{e=} \begin{cases} 8.1exp\left(-\frac{(\lambda-1.531)^2}{0.00078}\right), & 1.4 < \lambda \leq 1.55 \\ 5.2exp\left(-\frac{(\lambda-1.55)^2}{0.00078}\right), & 1.55 < \lambda \leq 1.6 \end{cases}$$

These formula can be used to find value of $\sigma_p\,(\nu_p)$, $\sigma_e\,(\nu_s)$ and $\sigma_a\,(\nu_s)$ for equations 4.4, 4.5 and 4.6.

4.4.2 Noise

Similar to that of SOA in EDFA also ASE noise is generated. The rate equation governing ASE noise signal power $P_{ase}(z, \nu_i)$ is [17]

$$\frac{dP_{ASE}(z,\nu_i)}{dz} = \gamma_a(z,\nu_i)\left[P_{ASE}(z,\nu_i) + P_0\right] - \gamma_a(z,\nu_i)P_{ASE}(z,\nu_i) \quad (4.7)$$

where P_0 represent the equivalent input noise power corresponding to one photon per mode in bandwidth ΔB

$$P_0 = h\nu_i \Delta B \quad (4.8)$$

ASE noise is found by solving equation 4.7, with equation 4.2 and equation 4.3 using equation 4.8

4.5 Model for Loop

4.5.1 Fiber Loop Without Header Replacement Mechanism

The Figure 2.12 shows the basic scheme. Here length of fiber plus EDFA should be equal to the length of one cell period i.e. equal to 53 bytes.

When cell circulates in the loop, the following effects occur [18]

- Loss takes place in the signal due to fiber, coupler, WDM demultiplexer and Multiplexer in each rotation. Simultaneously signal is amplified due to SOA and EDFA gain.
- During each rotation more ASE noise due to SOA and EDFA is generated. Also the ASE noise generated in earlier rotations get amplified (due to gain of SOA and EDFA) as well as reduced (due to loss in fiber coupler, WDM demultiplexer and multiplexer).

If total number of rotations in the loop is N and the number of channels is M then above effects can be represented in following mathematical form

-After n^{th} rotation output signal power $P_{o,n}$ (dBm) is given by

$$P_{o,n} = P_{o,n-1} - \lceil \log_2 M \rceil \times 3.5 + G_{soa,n}(\lambda) - \lceil \log_2 M \rceil \times 3.5 - 0.2 \times l + G_{edfa,n}(\lambda) - 3.5 \qquad n > 0$$

where $P_{o,n-1}$ is output power after $(n-1)^{th}$ rotation, second term represents loss due to demultiplexer, third term is gain due to SOA, fourth term is loss due to multiplexer, fifth term is loss due to fiber, sixth term is gain due to EDFA and seventh term is loss due to coupler. The $P_{o,0}$ is given by

$$P_{o,0} = P_{in} - 3.5 \qquad n = 0$$

In the above equations l $(m\ km)$ is the length of fiber in loop.

-ASE noise due to SOA.

The contribution of ASE noise power generated at n^{th} rotation after the N rotations is given by

$$\begin{aligned} ASE_{soa,n}(\lambda) = {} & ASE^{o}_{soa,n}(\lambda) - \lceil \log_2 M \rceil \times 3.5 - 0.2 \times l + G_{edfa,n}(\lambda) - 3.5 \\ & + \sum_{i=n+1}^{N} \{ - \lceil \log_2 M \rceil \times 3.5 + G_{soa,i}(\lambda) - \lceil \log_2 M \rceil \times 3.5 \\ & - 0.2 \times l + G_{edfa,i}(\lambda) - 3.5 \} \end{aligned}$$

where $ASE^{o}_{soa,n}(\lambda)$ is the ASE noise generated by SOA in the n^{th} rotation. Therefore total ASE noise due to SOA after N^{th} rotation will be

$$ASE_{soa}(\lambda) = \sum_{i=1}^{N} ASE_{soa,i}(\lambda) \qquad mw$$

In the above equation the summation is done after converting $ASE_{soa,i}(\lambda)$ into mw

- ASE noise due to EDFA:

Contribution of ASE noise generated in n^{th} rotation, after the N rotations is given by

$$ASE_{edfa,n}(\lambda) \quad ASE^{n}_{edfa,n}(\lambda) - 3.5 + \sum_{i=n+1}^{N} \{-\lceil \log_2 M \rceil \times 3.5 + G_{soa,i}(\lambda) - \lceil \log_2 M \rceil \times 3.5 - 0.2 \times l + G_{edfa,i}(\lambda) - 3.5\}$$

where $ASE^{n}_{edfa,n}(\lambda)$ is the ASE noise generated by EDFA in the n^{th} rotation. Therefore total ASE noise due to EDFA after N rotations is given by

$$ASE_{edfa}(\lambda) = \sum_{i=1}^{N} ASE_{edfa,i}(\lambda) \qquad mw$$

In the above equation the summation is done after converting $ASE_{edfa,i}(\lambda)$ into mw

In above discussion it should be noted that gain of SOA and EDFA depend on the particular rotation simply because of the fact that input power to SOA and EDFA depend on that particular rotation

After N rotations

$$Noise = ASE_{soa}(\lambda) + ASE_{edfa}(\lambda)$$

Thus $$SNR = \frac{P_{in,N}}{Noise}$$

4.5.2 Fiber Loop With Header Replacement Mechanism

The diagram for this is shown in Figure 3.7 The model for this loop is simply an extension of the model in Section 4.6.1 As mentioned in Section 3.4, the length of loop should be equal to the length of 53 bytes

when the cell circulates in the loop, following effects occur

- Loss takes place in the signal due to fiber, couplers, splitters WDM demultiplexer and multiplexer in each rotation Simultaneously gain also occur due to SOA and EDFA in each rotation
- During each rotation, more ASE noise due to SOA and EDFA as well as more crosstalk noise, due to SOA (of header replacement mechanism) is generated Also the ASE noise and crosstalk noise generated in earlier rotations gets amplified (due to gain of SOA and EDFA) as well as reduced (due to loss in fiber, coupler, splitter WDM demultiplexer and multiplexer)

Consider the combined loss due to 10 dB splitter and 3 dB splitter of header replacement mechanism See Figure 4 6

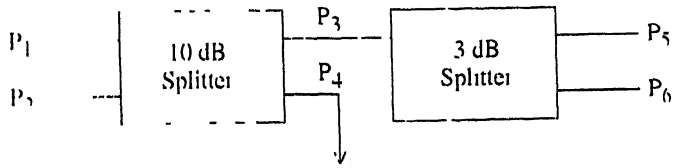


Figure 4 6: 10 dB and 3 dB Splitter combined

Let power be given through port 1 and no input power at port 2 then for 10 dB splitter

$$\begin{aligned} -10\log_{10}\frac{P_1}{P_3+P_1} &= 10 \\ \Rightarrow \qquad P_1 &= \frac{P_3}{9} \end{aligned}$$

assume $P_1 = P_3 + P_1 \quad \Rightarrow P_3 = \frac{9P_1}{10}$.

For 3 dB splitter

$$-10\log\frac{P_5}{P_5+P_6} = 3$$
$$\Rightarrow \quad P_5 = P_6$$

since $P_3 \quad P_5 + P_6 \quad \Rightarrow P_5 = \frac{P_3}{10} = \frac{9P_1}{20}$

So combined loss due to 10 dB splitter and 3 dB splitter

$$loss \quad 10\log_{10}\frac{P_1}{P_5} = 10\log_{10}\frac{20}{9} = 3\ 47\ d\mathbf{B}$$

Now if we consider excess loss (0 5 dB) of both splitter then combined loss is given by

$$loss = 3.47 + 2 \times 0\ 5 = 4\ 47\ d\mathbf{B}$$

Consider the effect of rotation in the loop If total number of rotations in the loop is N and the number of channels is M then the effect of rotation of cell in the loop can be represented in following mathematical form

- After n^{th} rotation output signal power

$$P_{o\,n} = P_{o\,n-1} - \lceil\log_2 M\rceil \times 3\ 5 - 4.47 + G_{soa,n}(\lambda) - 3\ 5 - \lceil\log_2 M\rceil \times 3\ 5$$
$$0\ 2 \cdot l + G_{edfa,n}(\lambda) - 3\ 5, \qquad n > 0$$

where $P_{o\,n}$ is the output power after n^{th} rotation, second term represents loss due to WDM demultiplexer, third term is combined loss of 10 dB splitter and 3 dB splitter, fourth term is gain due to SOA, fifth term is the loss due to 3 dB coupler of header replacement mechanism, sixth term is loss due to WDM multiplexer, seventh term is loss due to fiber, eighth term is gain due to EDFA and ninth term is loss due to 3 dB coupler of the loop

$$P_{o,0} = P_{in} - 3.5 \qquad n = 0$$

where l (km) is the length of fiber in loop and P_{in} and $P_{o,l}$ are in dBm

- ASE noise due to SOA

ASE noise after N rotations due to n^{th} rotation

$$ASE_{soa,n}(\lambda) \qquad ASE^{o}_{soa,n}(\lambda) - 3.5 - \lceil \log_2 M \rceil \times 3.5 - 0.2 \times l + G_{edfa,n}(\lambda) - 3.5 + \sum_{i=n+1}^{N} \{ - \lceil \log_2 M \rceil \times 3.5 - 4.47 + G_{soa,i}(\lambda) - 3.5 - \lceil \log_2 M \rceil \times 3.5 - 0.2 \times l + G_{edfa,n}(\lambda) - 3.5 \}$$

where $ASE^{o}_{soa,n}$ is the original ASE noise generated due to SOA at the n^{th} rotation in dBm.

So total ASE noise due to SOA

$$ASE_{soa}(\lambda) = \sum_{i=1}^{N} ASE_{soa,i}(\lambda) \qquad mw$$

In above equation the summation is done after converting $ASE_{soa,i}$ into mw.

- ASE noise due to EDFA

ASE noise after N rotation due to n^{th} rotation

$$ASE_{edfa,n}(\lambda) \quad = \quad ASE^{o}_{edfa,n}(\lambda) - 3.5 + \sum_{i=n+1}^{N} \{ - \lceil \log_2 M \rceil \times 3.5 - 4.47 + G_{soa,i}(\lambda) - 3.5 - \lceil \log_2 M \rceil \times 3.5 - 0.2 \times l + G_{edfa,n}(\lambda) - 3.5 \}$$

where $ASE^{o}_{edfa,n}(\lambda)$ is the original ASE noise generated due to EDFA at the n^{th} rotation.

So total ASE noise due to EDFA

$$ASE_{edfa}(\lambda) = \sum_{i=1}^{N} ASE_{edfa,i}(\lambda) \qquad mw$$

In the above equation the summation is done after changing $ASE_{edfa,i}(\lambda)$ in mw

- Crosstalk noise due to SOA in header replacement mechanism

In header replacement mechanism one of the two SOAs remains on at a time while other remains off. The signal passing the respective SOAs experiences the gain G_{on} or G_{off}. Even during off state the signal with gain G_{off} ($\frac{G_0}{R_e}$ which is quite small)[2] passes through SOA, which acts as crosstalk noise in original signal passing through other SOA. Note it is like noise because the signal in one of the arms containing SOA in header replacement mechanism experiences some delay.

The effective crosstalk noise after N rotations for the crosstalk noise generated in n^{th} rotation is

$$\begin{aligned} CT_{soa,n}(\lambda) \qquad & CT^{o}_{soa,n}(\lambda) - 3.5 - \lceil \log_2 M \rceil \times 3.5 - 0.2 \times l + G_{edfa,n}(\lambda) - 3.5 \\ & + \sum_{i=n+1}^{N} \{ - \lceil \log_2 M \rceil \times 3.5 - 4.47 + G_{soa,i}(\lambda) - 3.5 \\ & - \lceil \log_2 M \rceil \times 3.5 - 0.2 \times l + G_{edfa,i}(\lambda) - 3.5 \} \end{aligned}$$

where

$$CT^{o}_{soa,n}(\lambda) = P_{in,soa,n}(\lambda) \times \frac{G_0}{R_e}$$

$P_{in,soa,n}(\lambda)$ is the input power to SOA in the n^{th} rotation

So total crosstalk noise due to SOA

[2]See Section 4.3

$$CT_{soa}(\lambda) = \sum_{i=1}^{N} CT_{soa,i}(\lambda) \qquad mw$$

In the above equation the summation is done after converting $CT_{soa,i}(\lambda)$ in mw

Thus after N rotations

$$Noise \qquad ASE_{soa}(\lambda) + ASE_{edfa}(\lambda) + CT_{demux}(\lambda) + CT_{soa}(\lambda)$$

Thus $$SNR = \frac{P_{out}}{Noise}$$

This chapter gives the mathematical formulation for the loop with and without header replacement mechanism Next chapter gives the result of computation based on these formulations

Chapter 5

Results and Analysis

In this chapter the results of performance analysis of the switch with header replacement mechanism (proposed in Section 3.4) are presented. These results are compared with those for the switch without header replacement mechanism (described in Section 2.4.6). The results are based on the computation model using different components in the loop described in Chapter 4. This study focuses on the Signal to Noise Ratio (SNR) at the output of the optical loop of the switch. Initially a very simplified form of optical loop has been considered which does not have EDFA and loss due to WDM demultiplexer, multiplexer and fiber are neglected. Later the computational analysis of loop is done considering all the components and their effects.

5.1 Broad Parameters of the Switch

In this Section some parameters of switch which are used in computation are presented.

5.1.1 Length of Loop

In order to find the length of the loop we need to know the following

$$\begin{aligned} Data\,rate &= 2.5\ Gbps \\ Payload\,size &= 48\ bytes \\ Header\,size &= 5\ bytes \end{aligned}$$

There the cells which are to be stored in the fiber loop will be of 53 bytes. As a consequence the length of loop should correspond to 53 bytes (explained in Section 3.4). Assuming the refractive index of fiber as 1.5 the loop length is $(53 \times 8) \times (2 \times 10^8)/(2.5 \times 10^9) \approx 34$ meters

5.1.2 Wavelength Range

The wavelengths used are between 1.525 μm to 1.535 μm. The maximum number of channels can be 5 because the channel spacing should be at least 2 nm.

As described in Section 1.3.1 the gain of EDFA is crucially dependent on the absorption and the emission cross-section area of EDFA at pump and signal wavelengths. It can be seen from Figure 4.5 that the absorption and the emission cross-section area of EDFA is approximately constant between the wavelengths 1.525 μm to 1.535 μm and is taken to be that at 1.530 μm.

5.1.3 Other Conditions

While doing computational analysis no effort has been made to limit the output power level equal to that of input power level. It is assumed that packets in the different channels are input to loop simultaneously and taken out simultaneously.

5.2 Computation for the Switch when FOLM does not have EDFA

It is very simplified form of the loop It is shown in Figure 5 1 and 5 2 Here losses due to Demultiplexer, Multiplexer and fiber of loop have been neglected Only gain ASE noise and crosstalk noise due to SOA has been considered This computation is considered only for a single channel The computation is done for both cases i e loop with and without header replacement

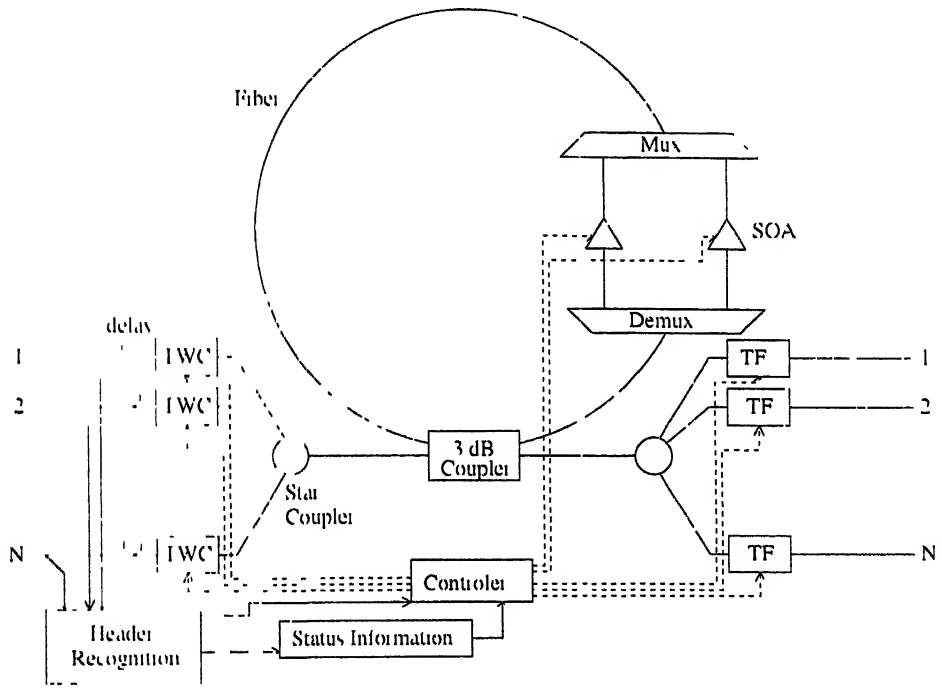


Figure 5 1 Switch without EFDA and header replacement mechanism

5.2.1 Specifications

With reference to the model of SOA described in Section 4 2. the parameter of SOA used are the following

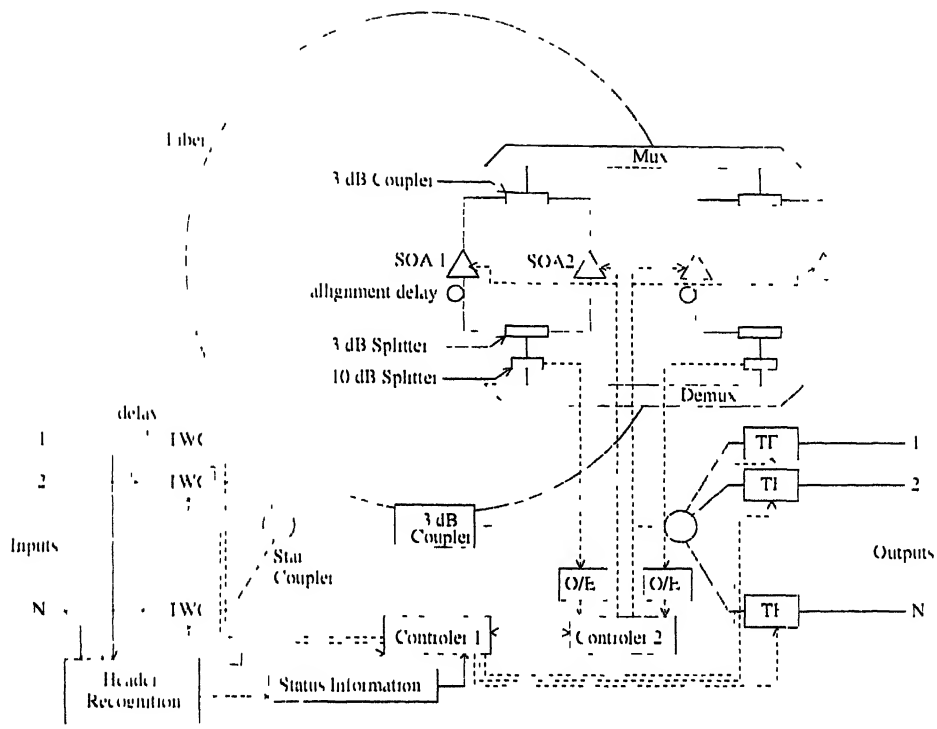


Figure 5.2 Switch with header replacement mechanism but without EDFA

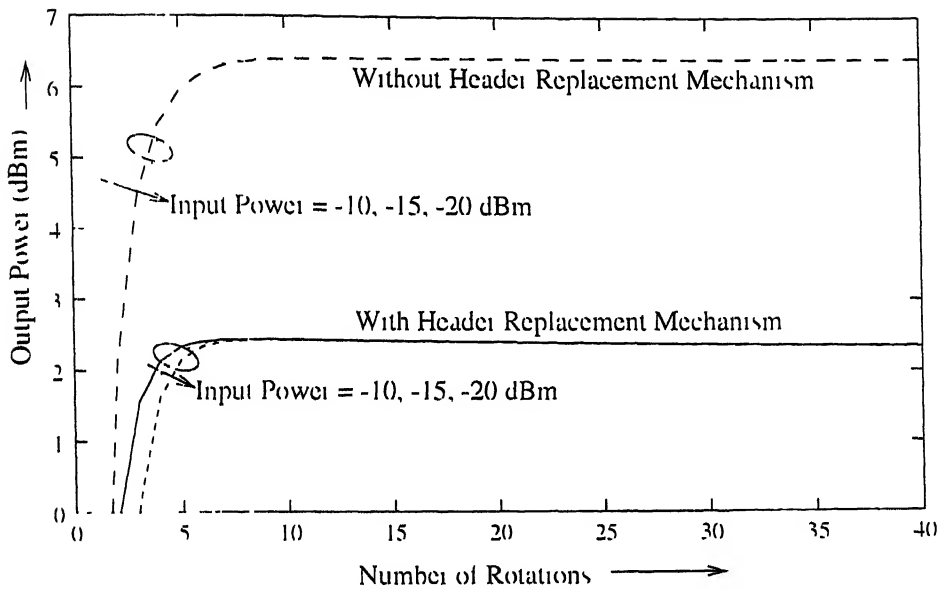


Figure 5.3 Output power vs Input Power for loop without EDFA and with or without header replacement mechanism for different input powers

for different input powers after few rotations It is due to the fact that crosstalk noise solely depends on the input power to SOA which becomes same after few rotations

Figure 5.6 shows that Signal to Noise Ratio (SNR) is considerably lower for loop with header replacement mechanism Obviously it is due to more noise generated for loop with header replacement mechanism Also for loop with header replacement mechanism, the SNR becomes approximately same for different input powers after few rotations. It is so because crosstalk noise is more prominent than ASE noise in this case and becomes same (Figure 5.5) after few rotations

Figure 5.7 shows that ASE noise is quite large in case of less input power Obviously it is due to the fact that at lower input power the ASE noise from SOA is more Figure 5.8 shows that SNR for lower input power is less than that for higher input power The same can also be concluded from Figure 5.7 Figure 5.8 shows that SNR decreases faster with increase in number of

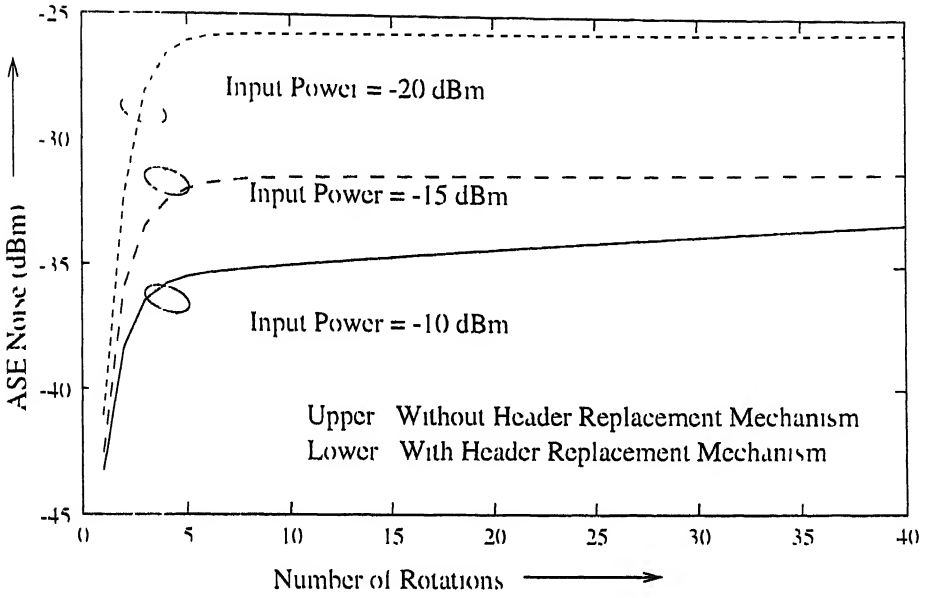


Figure 5.4 ASE noise vs Number of Rotations for loop without EDFA and with or without header replacement mechanism for different input powers

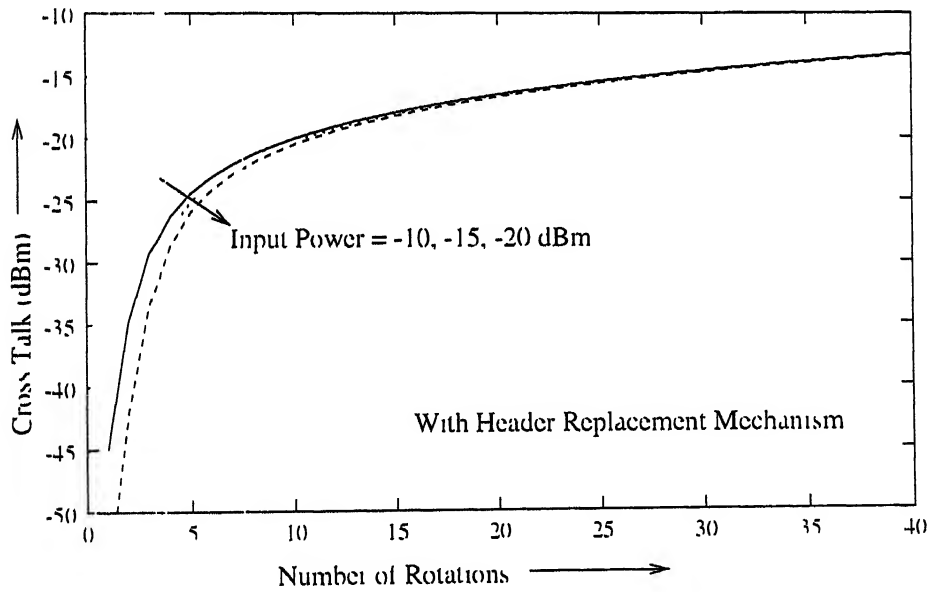


Figure 5.5. Crosstalk noise vs Number of Rotations for loop without EDFA and with header replacement mechanism for different input powers

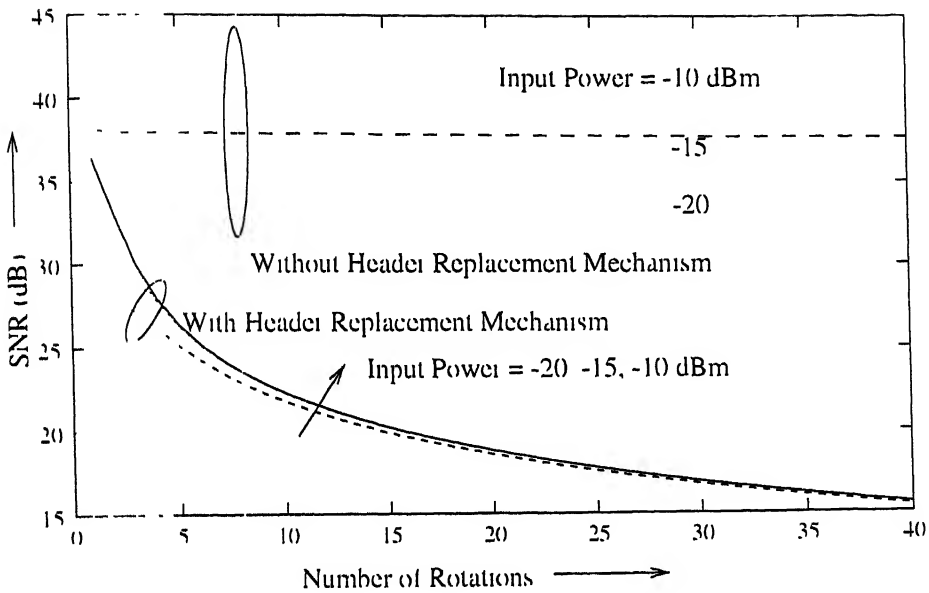


Figure 5.6 SNR vs Number of Rotations for loop without EDFA and with or without header replacement mechanism for different Input powers

rotations for loop with header replacement mechanism

5.3 Computation for the switch when FOLM has all components

The diagram for this case are shown in Figure 2.12 and 3.7. Here the final computation has been done for loop with and without header replacement mechanism. Here loss due to Demultiplexer, Multiplexer and fiber of loop has been considered. But the crosstalk noise due to demultiplexer has been neglected. The gain and ASE noise of EDFA has been considered.

5.3.1 Specifications

Following typical values of various parameters are used in computation

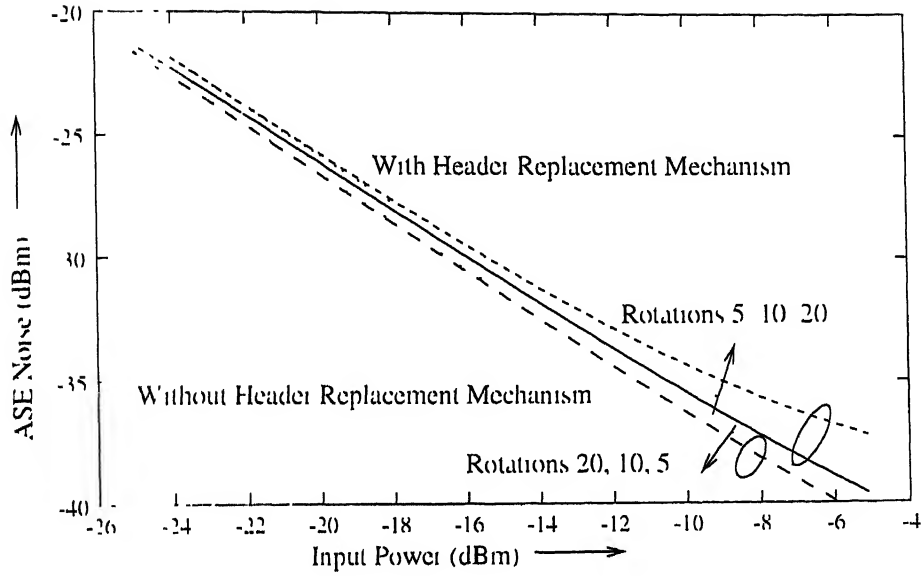


Figure 5.7 ASE noise vs. Input Power for loop without EDFA and with or without header replacement mechanism for different rotations

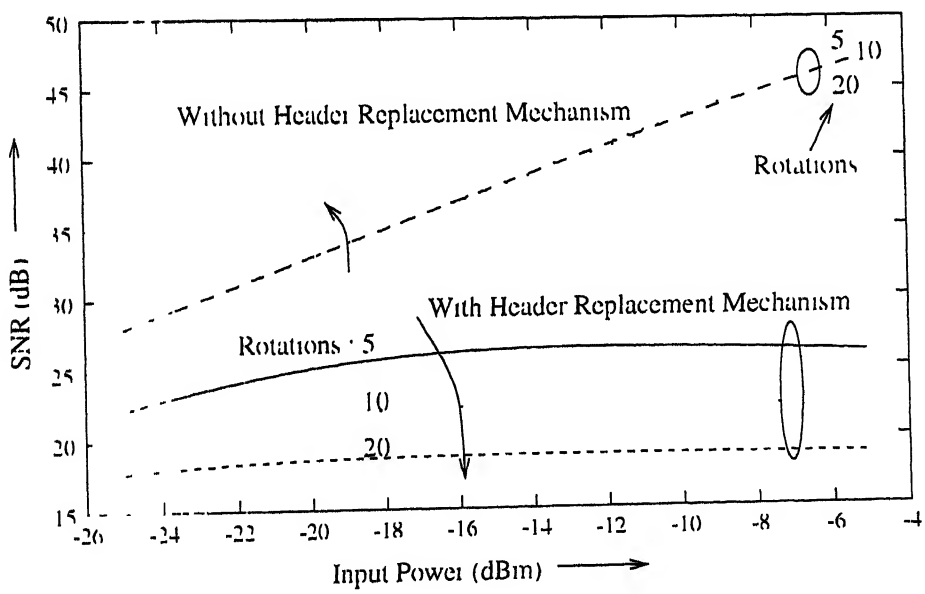


Figure 5.8 SNR vs. Input power for loop without EDFA and with or without header replacement mechanism for different input powers

1 *Loss due to Demultiplexer* $= 3.5 \times \lceil \log_2 N \rceil$[1]

2 *Loss due to Multiplexer* $= 3.5 \times \lceil \log_2 N \rceil$

3 *Fiber loss* $= 0.2$ *dB per km*

4 EDFA

a) *Level 2 to level 1 transition time* $\tau = 0.01$ *s*

b) *Mode radius* $= 2.5 \times 10^{-6}$ *m*

c) *Spot size* $\omega = 3.2 \times 10^{-6}$ *m*

d) *Density* $= 2.0 \times 10^{24}$ *per* m^3

e) *Spontaneous emission noise factor* $n_{sp} = 1.5$

f) *Pump power wavelength* $\lambda_p = 1.44$ *μm*

g) *Input pump power* $= 16.0$ *dBm*

Using the formulation as described in Chapter 4, the results are computed. In order to analyse the noise generated within the switch the input ASE noise and crosstalk for each channel is assumed to be zero. Also initially the input power to all channels is kept same. In such cases the output power, ASE noise and crosstalk noise for different channels vary very slightly.

5.3.2 Observations

As the number of channels increases, the loss due to Demultiplexer and Multiplexer increases significantly. After exceeding a certain number of channels this loss is too much and can not be compensated with gain of SOA. In the case of loop without header replacement mechanism such situation arises when the number of channels is more than four. Since loss in the loop with header replacement mechanism is more, number of channels can not exceed two. Under these circumstances it is necessary to use the EDFA which ultimately compensates the losses and more number of channels can be used.

[1] See Section 1.2

The result of computation has been presented in the form of graphs. Here output power, ASE/CT noise and SNR has been plotted vs. number of rotations, input power and EDFA length. Graphs are of two types, first when input power to all channels is same and second when input powers to all channels is different. In first case there are three kinds of graphs. In first kind output power, ASE/CT noise and SNR has been plotted with respect to number of rotations. In second kind they are plotted with respect to input power and in third kind with respect to EDFA length.

5.3.2.1 When Input Power to all Channels is Same

Graphs from Figure 5.9 to Figure 5.32 are under this category.

Output Power, ASE/CT Noise and SNR vs. Number of Rotations

Graphs from Figure 5.9 to Figure 5.14 are of this kind. The observation for the different graphs are following.

Figure 5.9 shows the output power level for different input power levels for loop with and without header replacement mechanism. It shows that after few rotations the output power level reaches to the same level irrespective of input power level. This Output power level is lower for loop with header replacement mechanism than that for loop without header replacement mechanism. It is due to the fact that loss in the loop with header replacement mechanism is more. Figure 5.9 also shows that for loop with header replacement mechanism if input power level is $-10\ dBm$ then output power level is less than that. Figure 5.10 shows that ASE noise for loop with header replacement mechanism is, in general, more than that for loop without header replacement mechanism. Also ASE noise is more for lower input power. For $-10\ dBm$ input power the ASE noise in initial few rotations is less for loop with header replacement mechanism than that for loop without header replacement mechanism. The reason for this is that for loop with header replacement mechanism the loss is large enough to suppress the ASE noise in initial few rotations. After these few rotations the ASE noise

generated itself becomes large. Figure 5.11 shows that ASE noise is more than crosstalk noise for loop with header replacement mechanism which is contrary to conclusion of Figure 5.4 and Figure 5.5. It is due to more loss in the loop.

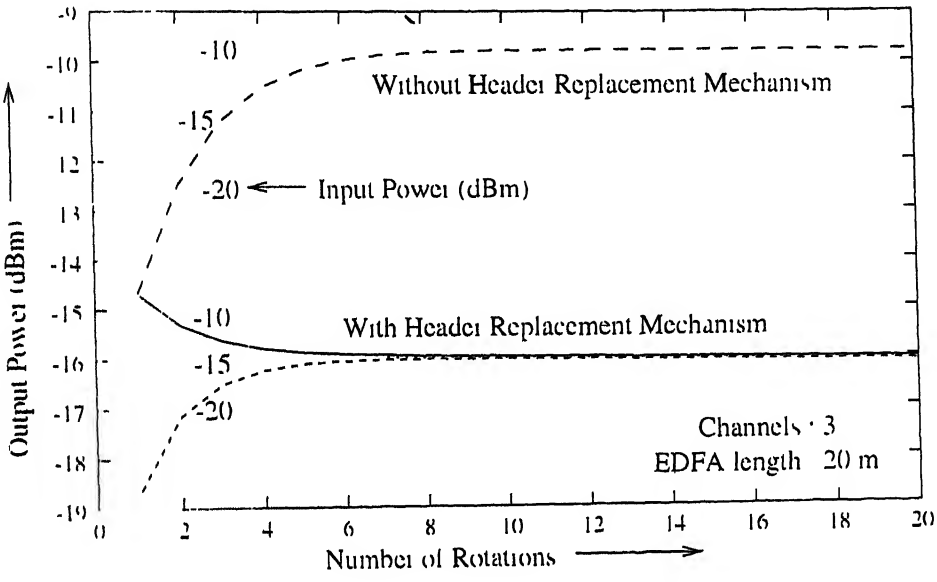


Figure 5.9 Output Power vs Number of Rotations for loop With and Without Header Replacement Mechanism for different input powers

Figure 5.12 shows that SNR for loop without header replacement mechanism is significantly more than that for loop with header replacement mechanism. At the same time the SNR for loop with header replacement mechanism is not very low and with the criterion of minimum SNR to be 10 dB, this loop can be used to store 3 channels even for more than 20 rotations.

Figure 5.13 shows that for 5 channels, the output power levels are quite low for both kind of loops. Also the output power level decreases after each successive rotations. It is so because the ASE noise generated in this case is significantly large. Figure 5.14 shows that the SNR is also low for both loops and with the criterion described above the loop with header replacement mechanism can be used to store 5 packets only for 4 *or* 5 rotations.

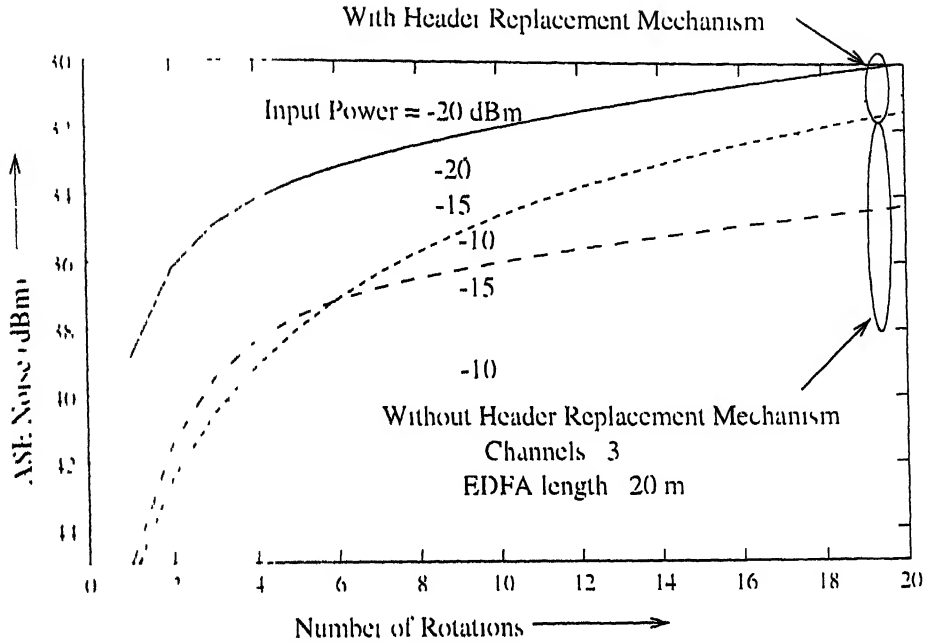


Figure 5.10 ASE noise power vs number of rotations for loops with and without header replacement mechanism for different input powers

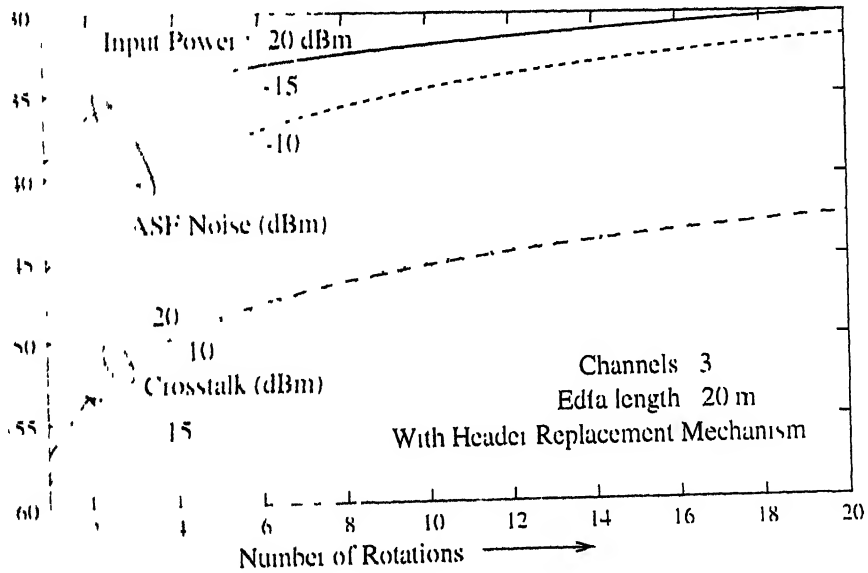


Figure 5.11 ASE noise power and Crosstalk noise vs Number of Rotations for loop with header replacement mechanism for different input power levels

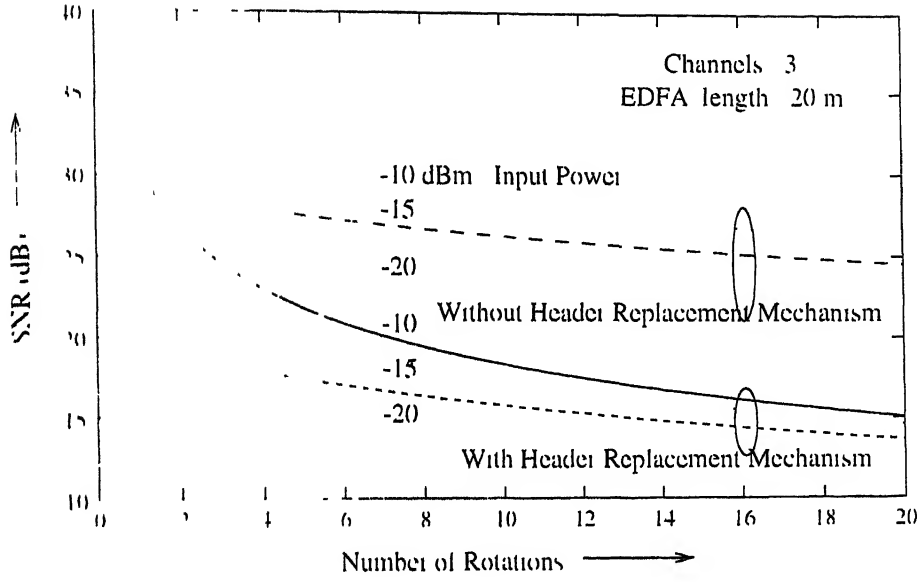


Figure 5.12: SNR vs. Number of Rotations with and without header replacement mechanism for different input power levels

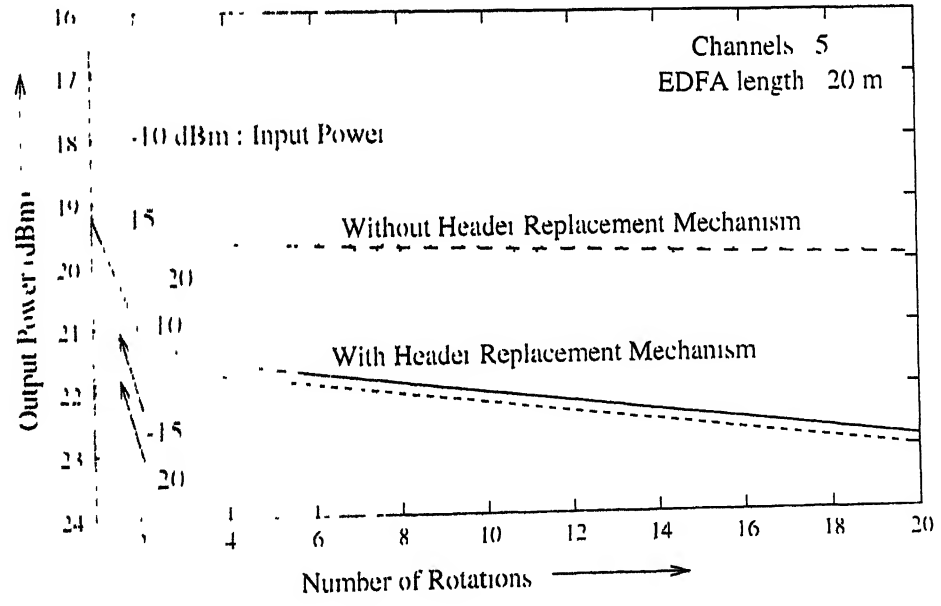


Figure 5.13: Output Power vs Number of Rotations for loop with and without header replacement mechanism for different input power levels

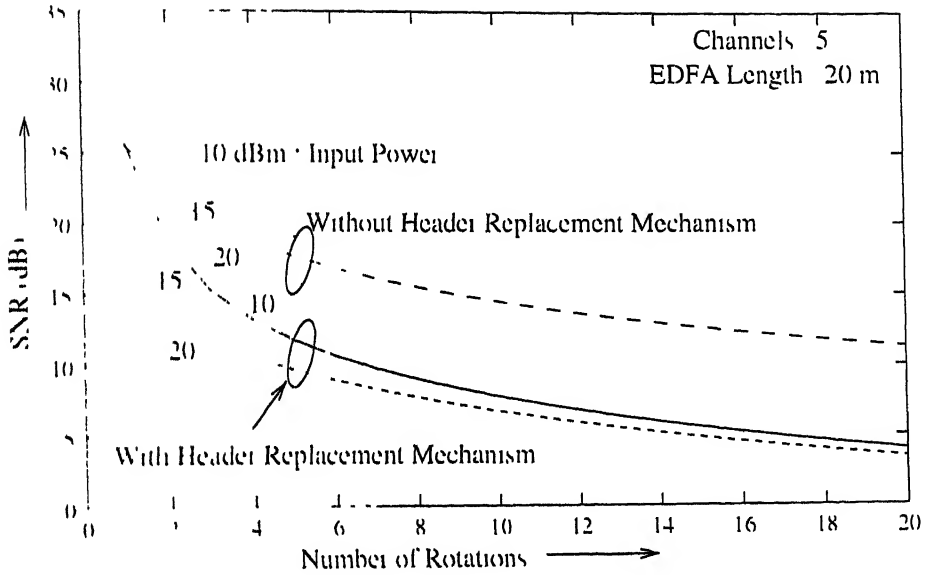


Figure 5.14: SNR vs Number of Rotations for loop with and without header replacement mechanism for different input power levels

Output Power, ASE/CT Noise and SNR vs. Input Power

Graphs from Figure 5.15 to Figure 5.24 are of this kind

Figure 5.15 and 5.16 shows that output power levels of the loop with and without header replacement mechanism does not vary much with the change in the input power (obviously it is the case after 5, 10, or 20 rotations. In the initial few rotations it varies significantly for different input powers as indicated by Figure 5.9 and Figure 5.13). But it changes very significantly for change in the number of the channels. Also for loop with header replacement mechanism the output power [illegible] faster. The same was also concluded from Figure 5.9 and Figure 5.13.

Figure 5.17 and Figure 5.18 shows that the SNR varies more significantly for the change in input power with less number of channels. It happens because for less number of channels, the decrease in ASE noise with increase of input power is more. These figures also shows that decrease in SNR with increase in number of rotations is more for loop with header replacement

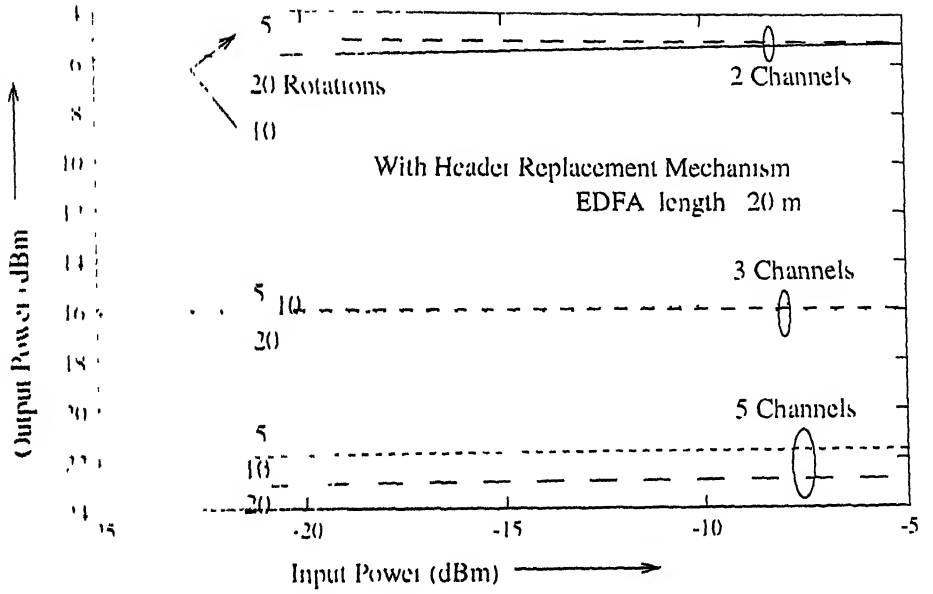


Figure 5.15: Output power vs Input power for loop with header replacement mechanism for different channels and rotations

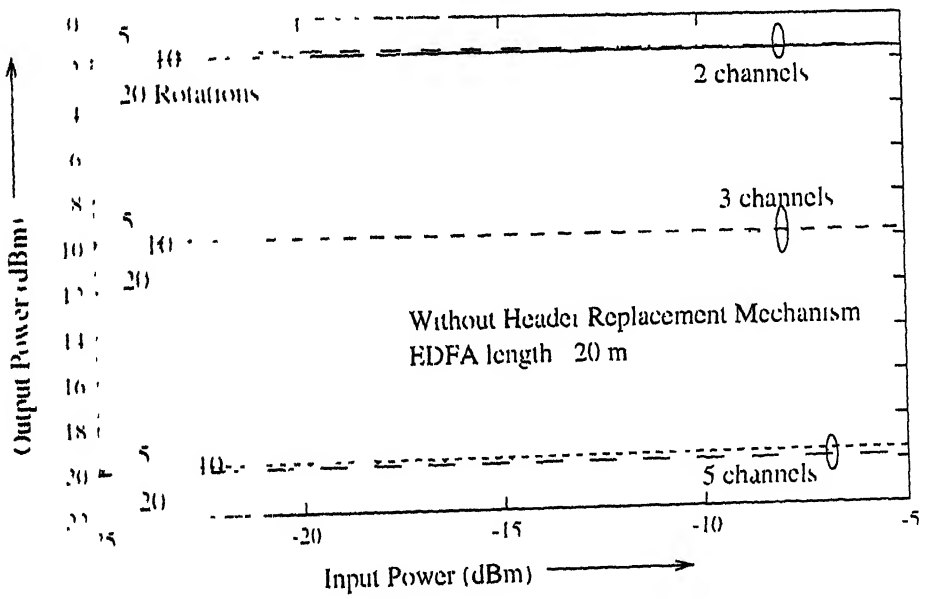


Figure 5.16: Output Power vs Input Power for loop without header replacement mechanism for different number of rotations

mechanism. Also the loop with header replacement mechanism can't be used to store 5 packets for 5 or more rotations.

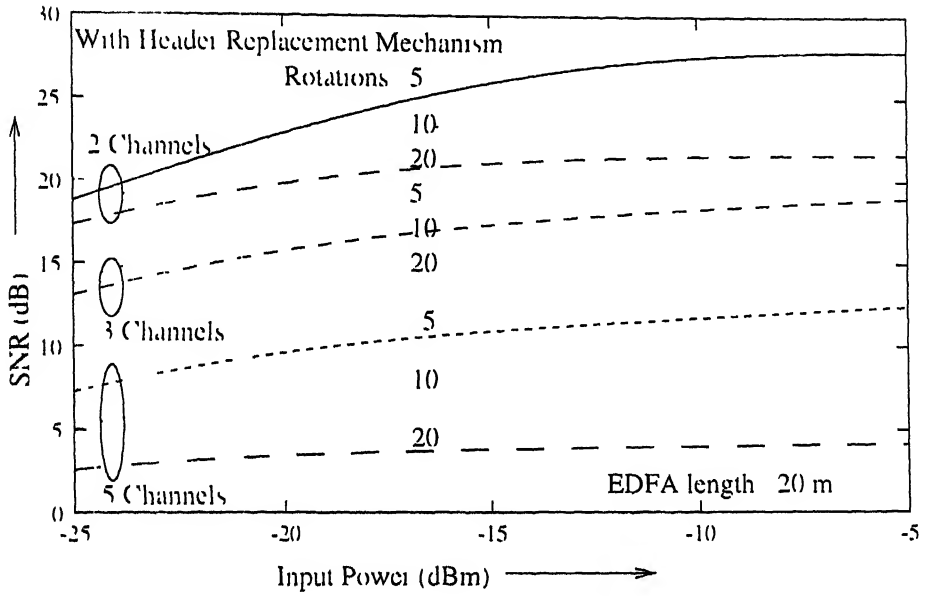


Figure 5.17 SNR vs. Input Power for loop with header replacement mechanism for different number of channels and rotations.

Figure 5.19 and Figure 5.20 shows that output power level changes significantly with EDFA length. Also for smaller EDFA lengths (and less number of rotations) the output power level changes more with the change in input power. It happens simply because of the fact that for smaller EDFA length, its gain is low. Figure 5.21 and Figure 5.22 shows that ASE noise for loop with header replacement mechanism is larger and it decreases with increase in input power. But the rate of decrease of ASE noise with increase in input power is more for less number of rotations. It is due to fact that some new ASE noise is added after each rotation. These figures also show that decrease of ASE noise with increase in input power is less for loop with header replacement mechanism than that for loop without header replacement mechanism. It is so because the loss in the loop with header replacement mechanism is more and hence the gain and ASE noise of loop's components is more.

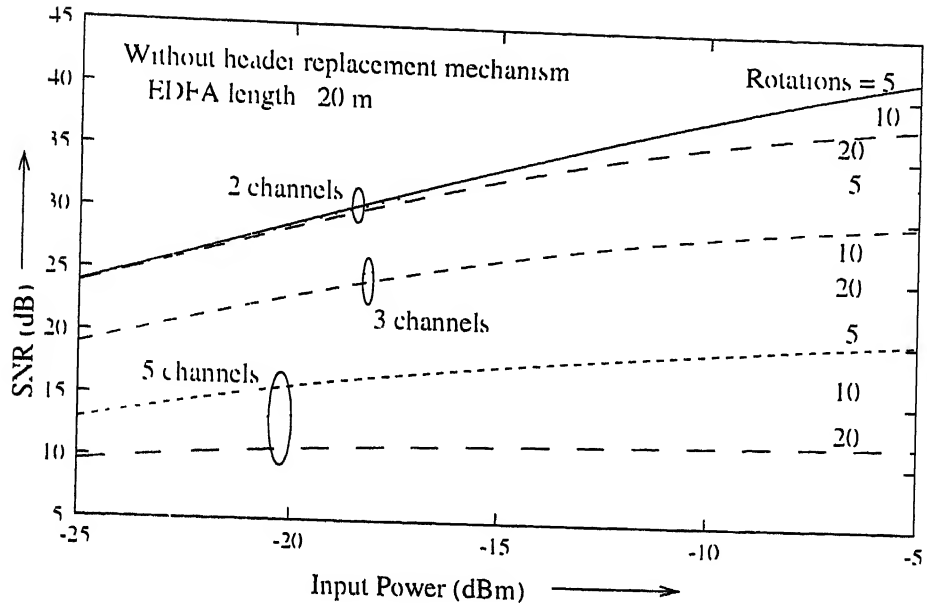


Figure 5.18: SNR vs Input power for loop without header replacement mechanism for different channels and rotations

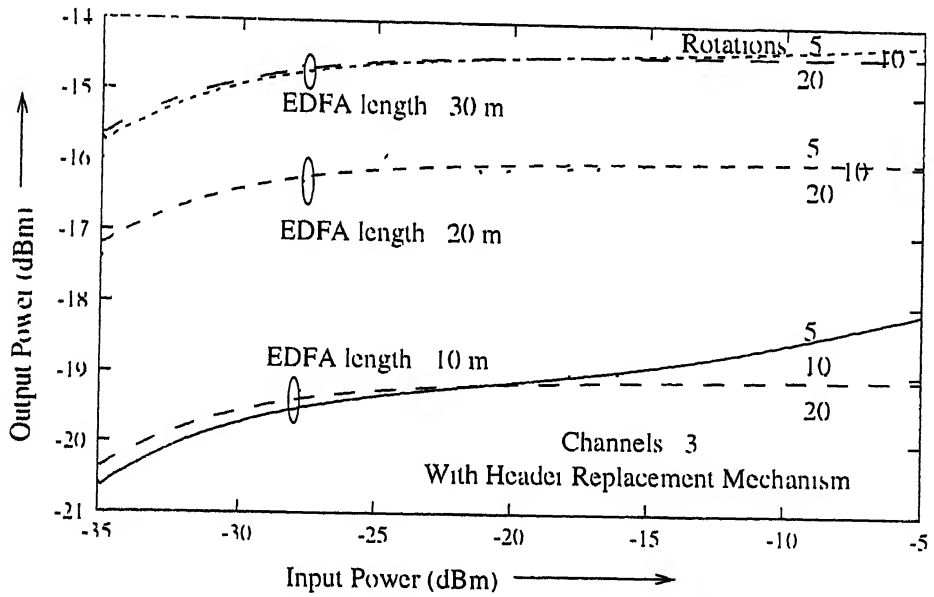


Figure 5.19 Output power vs Input Power for loop with header replacement mechanism for different EDFA lengths and rotations

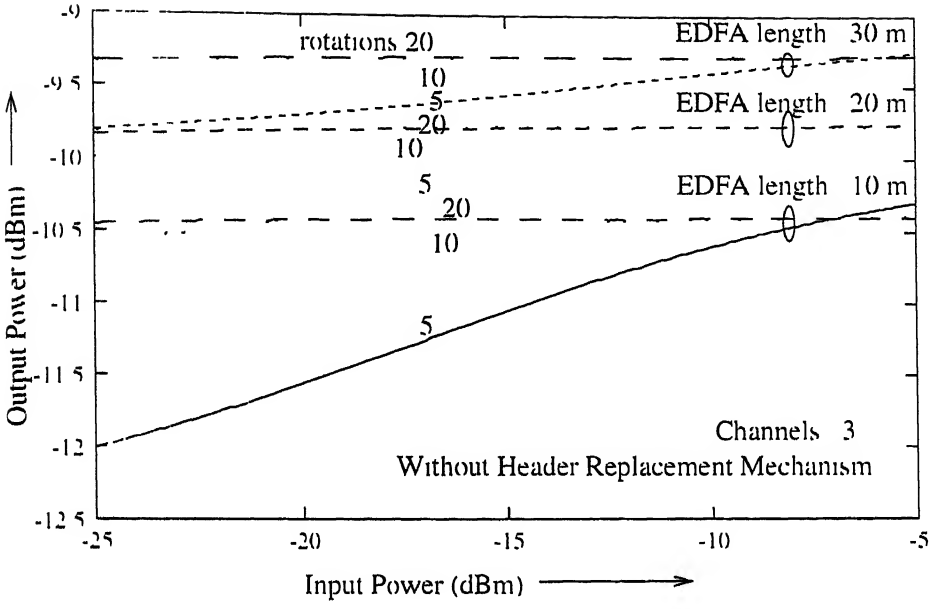


Figure 5.20 output power vs Input Power for loop without header replacement mechanism for different EDFA lengths and rotations

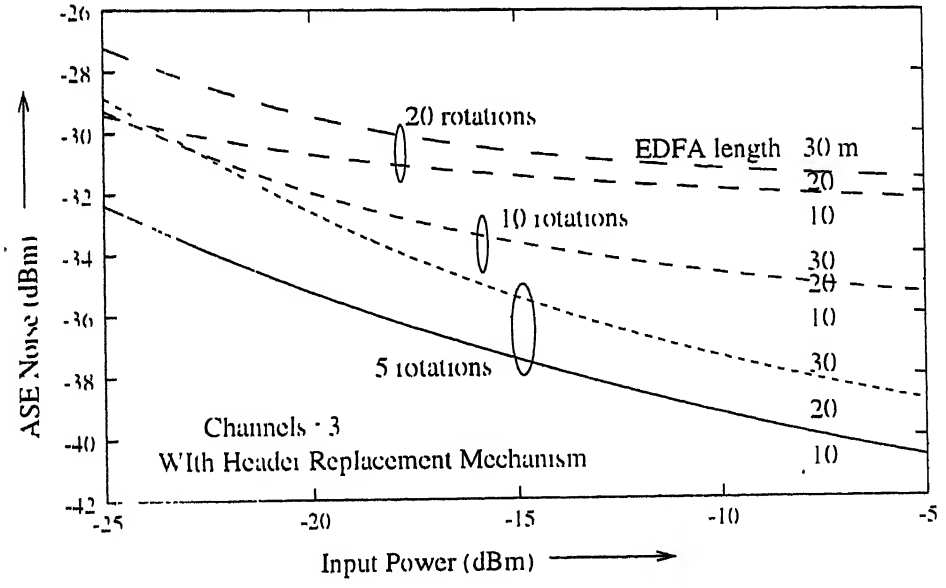


Figure 5.21 ASE noise vs Input Power for loop with header replacement mechanism for different EDFA lengths and rotations

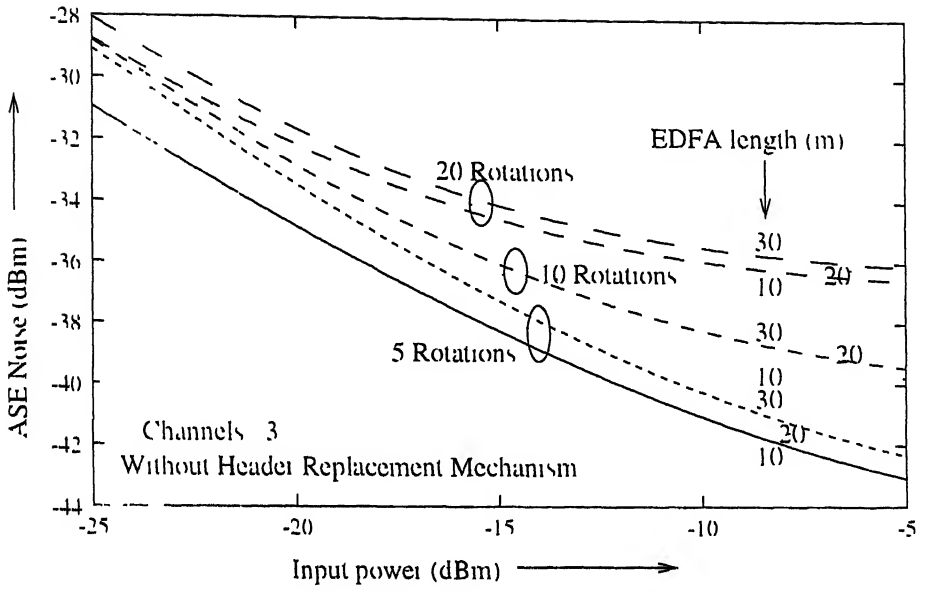


Figure 5.22 ASE noise vs Input Power for loop without header replacement mechanism for different EDFA lengths and rotations

Figure 5.23 and Figure 5.24 shows that SNR increases significantly with increase in input power. It decreases with increase in number of rotations and increases with increase in EDFA length. The effect of number of rotations is prominent at higher input power and the effect of EDFA length is prominent at lower input power (It is more so for loop with header replacement mechanism). It is because of more gain of EDFA at lower input power.

Output Power, ASE/CT Noise and SNR vs. EDFA length

Figure 5.25 shows that output power after 5 rotations increases with EDFA length. This effect is more prominent for the loop with header replacement mechanism. It is due to more loss in the loop. Also as the EDFA length increases the output power for different input powers becomes approximately same. Figure 5.26 shows that the increase of ASE noise with EDFA length is also faster for loop with header replacement mechanism. The reason for this is again more loss in loop with header replacement mechanism. Figure 5.27 shows that for loop with header replacement mechanism the crosstalk noise

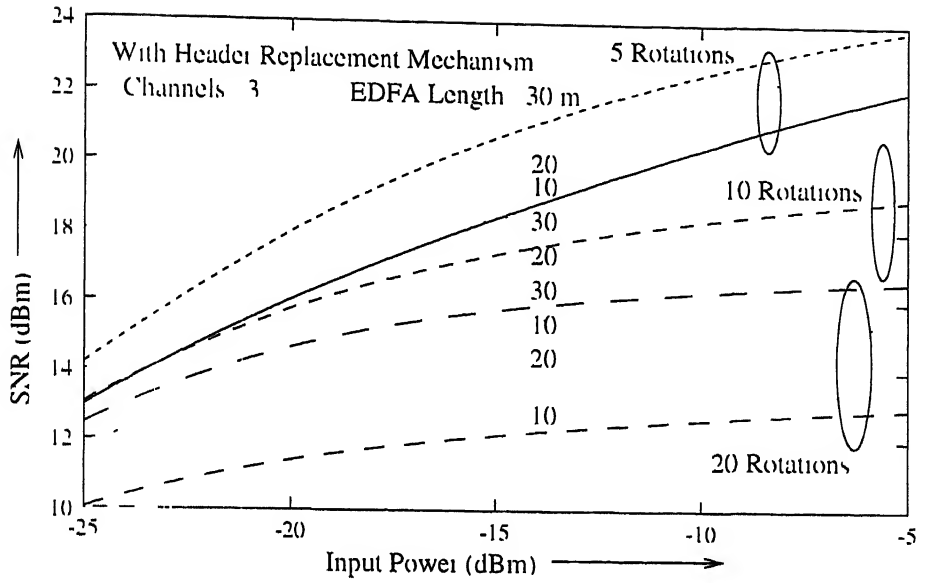


Figure 5.23 SNR vs Input Power for loop with Header replacement mechanism for different EDFA lengths and rotations

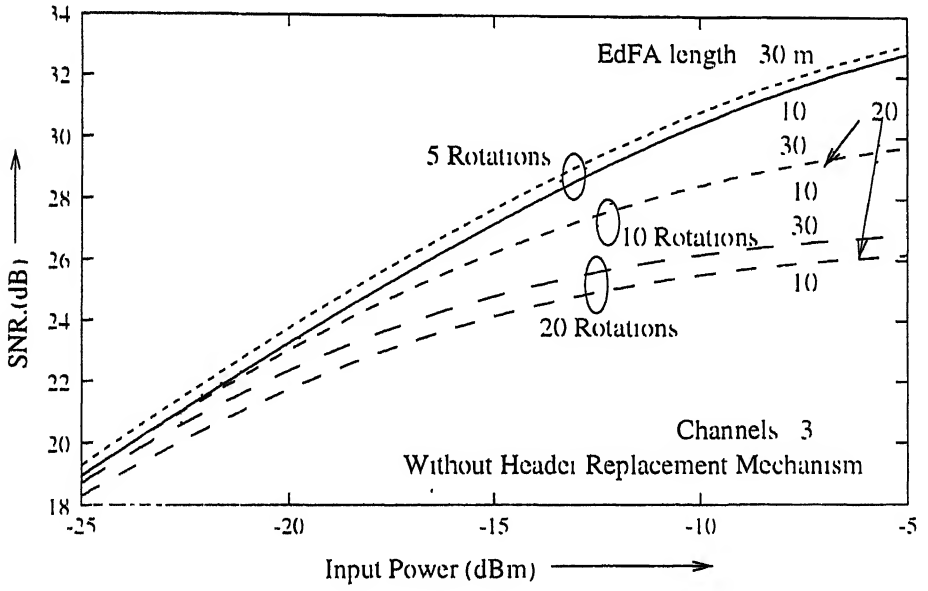


Figure 5.24 SNR vs Input Power for loop without header replacement mechanism for EDFA lengths and rotations

becomes approximately same as EDFA length increases while ASE noise remains significantly different. It is so because crosstalk noise is a direct result of output power and output power becomes approximately same as EDFA length increases.

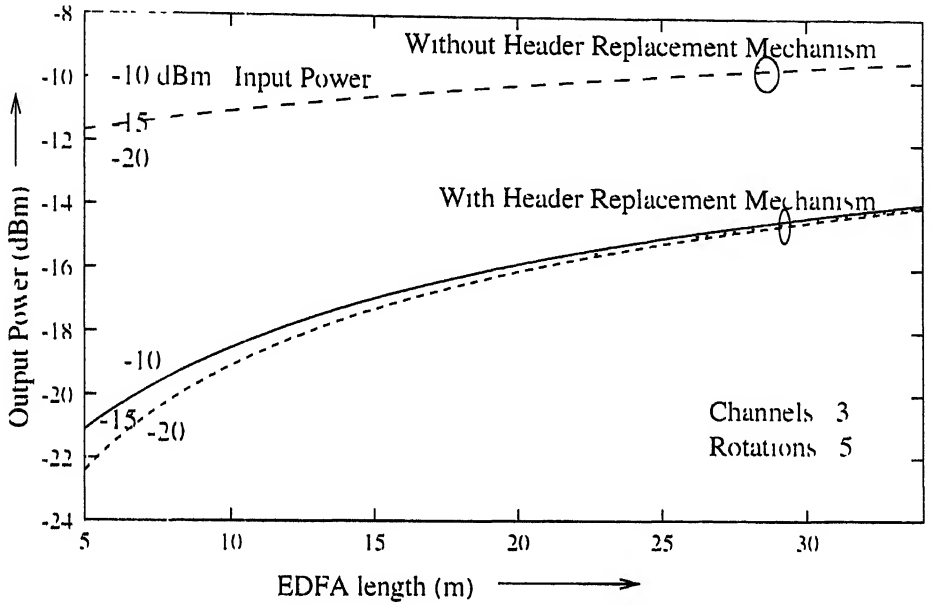


Figure 5.25 Output power vs. EDFA length for loop with and without header replacement mechanism for different input powers.

Figure 5.28 shows that SNR remains different irrespective of EDFA length for both cases i.e. for loop with and without header replacement mechanism. This effect is due to ASE noise (because even in the loop with header replacement mechanism ASE noise remains dominant over crosstalk noise, refer to Figure 5.27). Since SNR remains more than 10, the loops can be used with any EDFA length more than 5 meters.

Figure 5.29 shows that output power level after 10 rotations increases with EDFA length but it remains same for different input powers viz. $-10\ dBm$, $-15\ dBm$ and $-20\ dBm$. At the same time one can observe from Figure 5.30 that the SNR remains different even though it also increases with EDFA

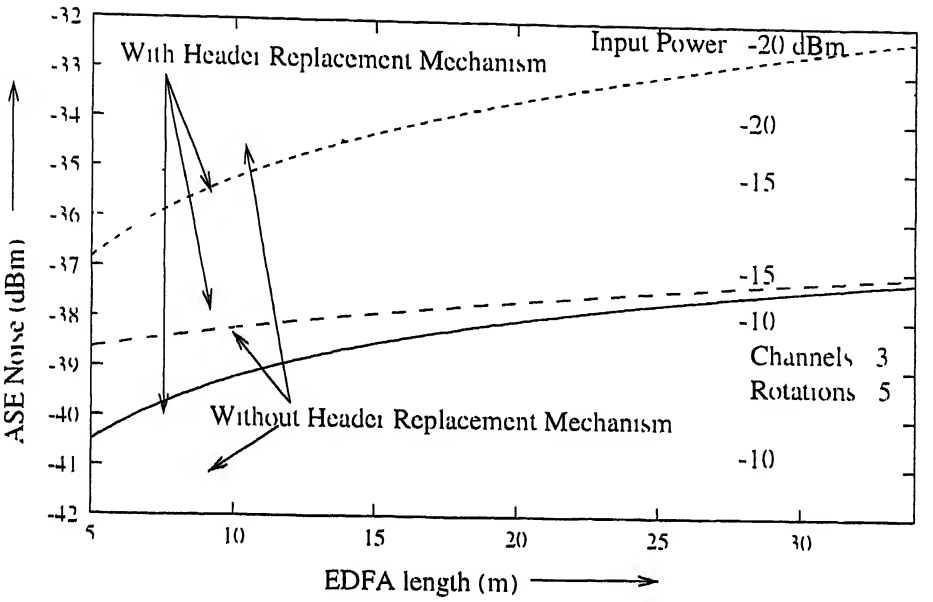


Figure 5.26: ASE noise vs EDFA length for loop with and without header replacement mechanism for different input powers

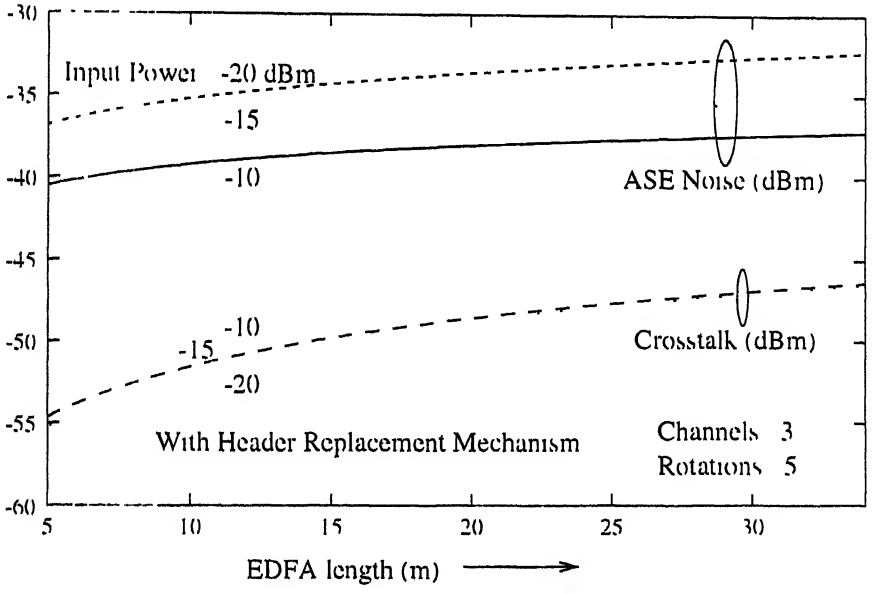


Figure 5.27: ASE noise and Crosstalk noise vs. EDFA length for loop with header replacement mechanism for different input powers

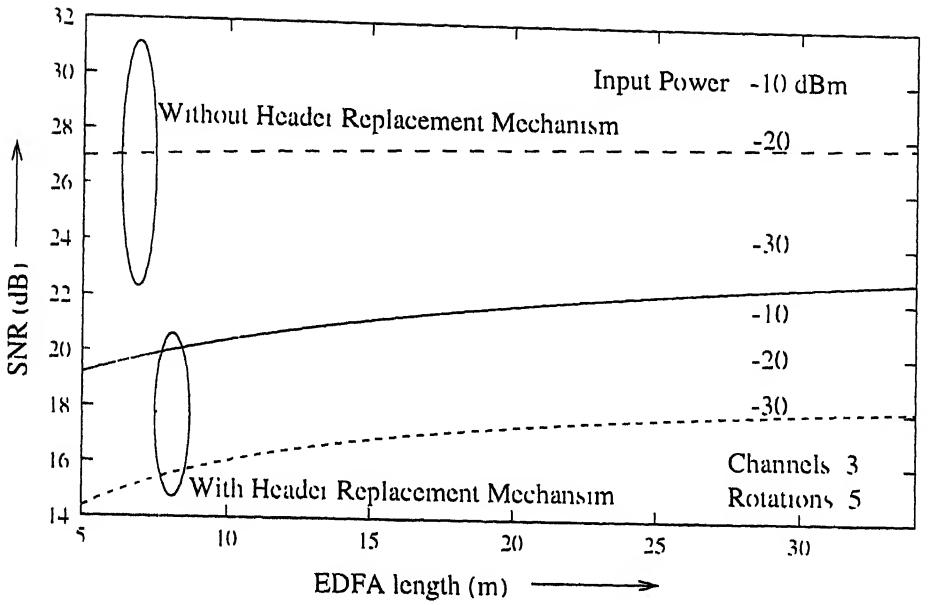


Figure 5.28 SNR vs EDFA length for loop with and without header replacement mechanism for different input powers.

length. Again this is due to effect of ASE noise.

Figure 5.31 shows that as the number of channels increases the output power decreases and effect of EDFA length becomes significant. It is basically due to more loss in the loop. This effect is clearly visible for the case of three channels in the loop with and without header replacement mechanism. Figure 5.32 shows that for large number of channels the SNR is very low and in case of loop with header replacement mechanism even the larger EDFA length does not make enough compensation for losses. Hence the loop with header replacement mechanism can't be used for 5 or more channels.

5.3.2.2 When Input Power to all Channels is Different.

Graphs from Figure 5.33 to Figure 5.36 are under this category.

Figure 5.33 shows the output power vs number of rotations when different power is sent to different channels. It shows that in this case also

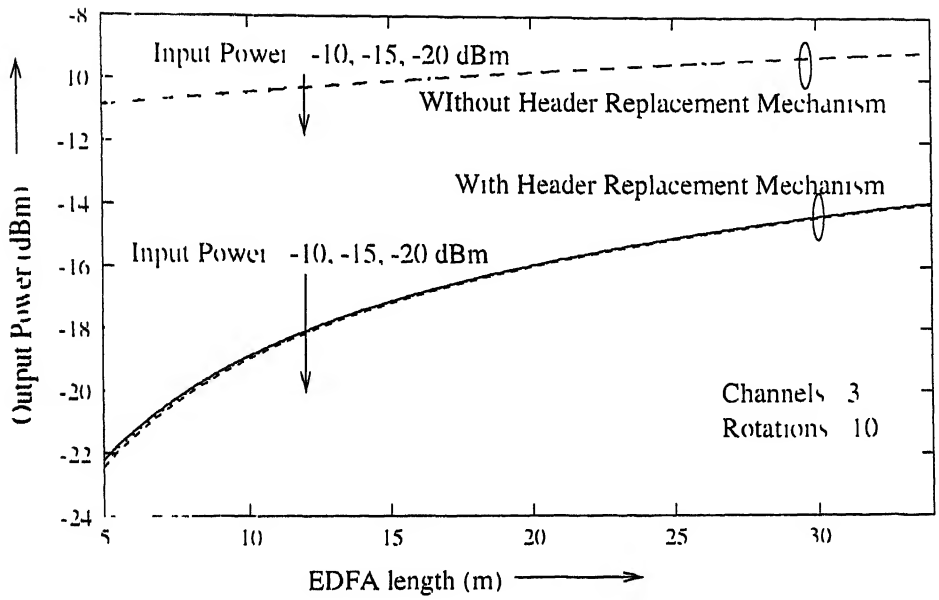


Figure 5.29: Output Power vs EDFA length for loop with and without header replacement mechanism for different input powers

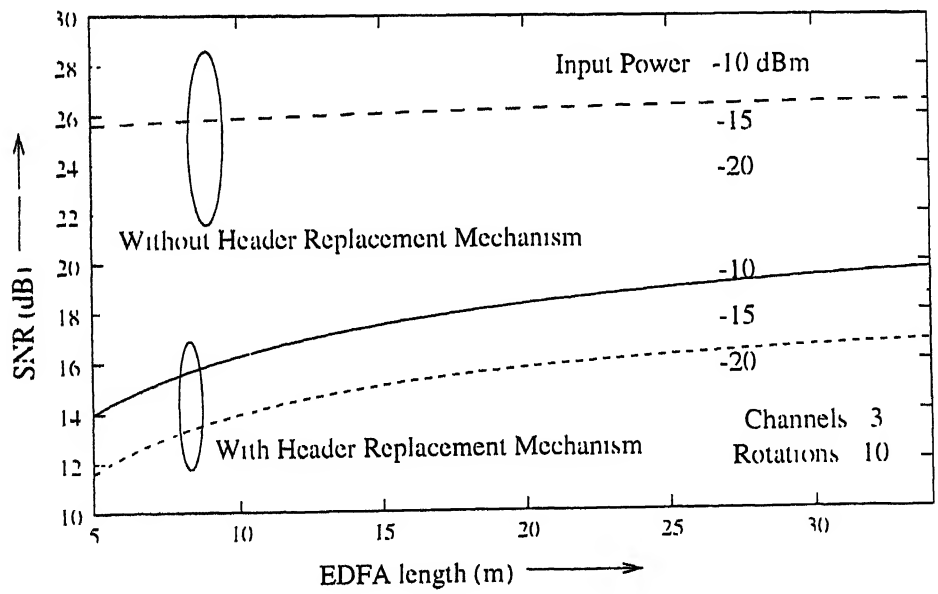


Figure 5.30: SNR vs EDFA length for loop with and without header replacement mechanism for different input powers

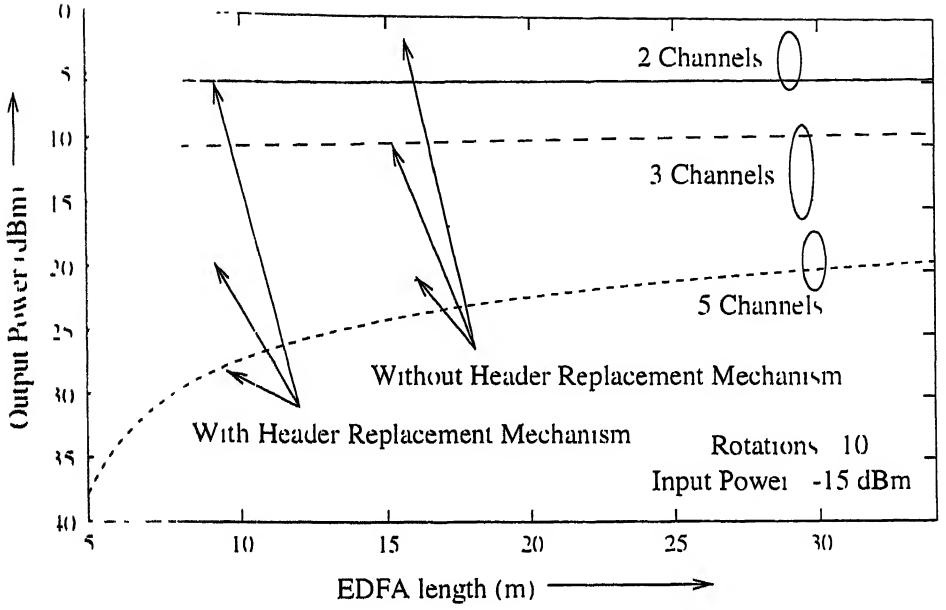


Figure 5.31 Output power vs EDFA length for loop with and without header replacement mechanism for different number of channels

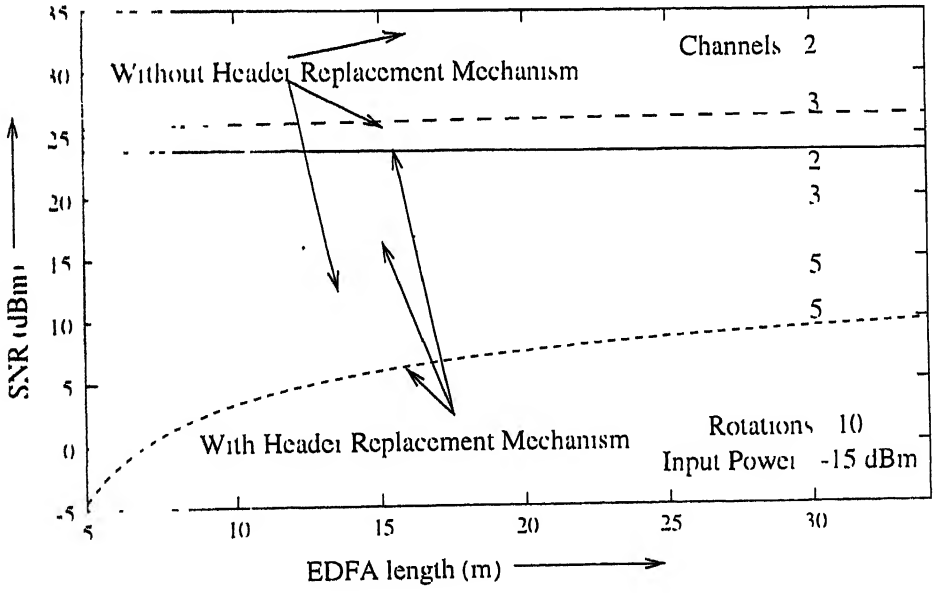


Figure 5.32 SNR vs. EDFA length for loop with and without header replacement mechanism for different number of channels

the output power tend to converge at same level It is easily visible for the loop without header replacement mechanism Obviously, due to more loss the output power level in case of loop with header replacement mechanism is lower than that for loop without header replacement mechanism Figure 5.34 also shows that the ASE noise for the channel with less input power is more It is due to more gain and hence more ASE noise of SOA After few rotations the ASE noise for loop with header replacement mechanism becomes more than that for loop without header replacement mechanism In the initial rotations for -20 dBm input power the ASE noise is more for loop without header replacement mechanism than that for loop with replacement mechanism. The reason for this is that when sum of powers of all channels is input to EDFA, the effective gain for the channel of least power is very small. Thus the channel of least power is amplified effectively only by SOA which compensates different losses in the loop -20 dBm is the least power among all the channels here As a result the signal remains very low and large ASE noise is produced every time, and thus ASE noise for this channel rises very fast But after few rotations the ASE noise for loop with header replacement mechanism becomes more

Figure 5.35 shows that crosstalk noise is quite less than ASE noise for different channels of loop with header replacement mechanism It is because of the significant loss in the loop Also for channel in which input power is least (channel 1), the ASE noise is highest and crosstalk noise is lowest It is something expected as per the explanations given earlier

Figure 5.36 shows that SNR for channels with more input power is more Obviously SNR is more for loop without header replacement mechanism than that for loop with header replacement mechanism Clearly if input power of a channel is too low then it can't be used in loop

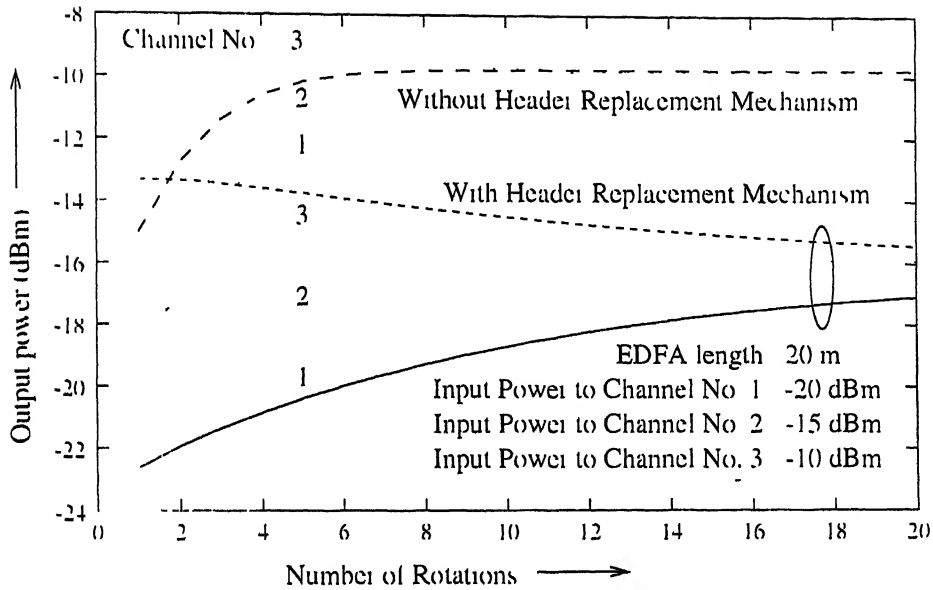


Figure 5.33: Output power vs Number of rotations for loop with and without header replacement mechanism for different input power to channels

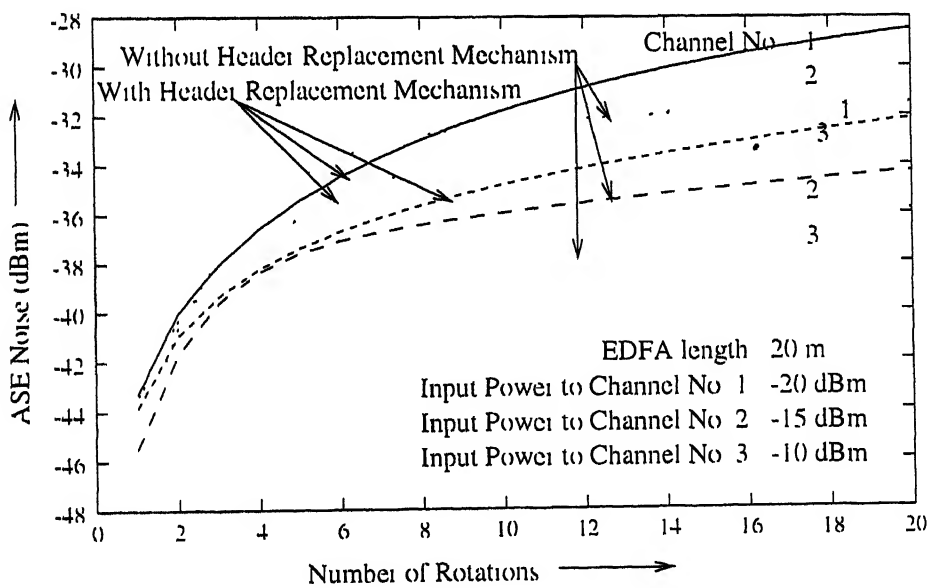


Figure 5.34 ASE noise vs Number of rotation for loop with and without header replacement mechanism for different input powers to channels.

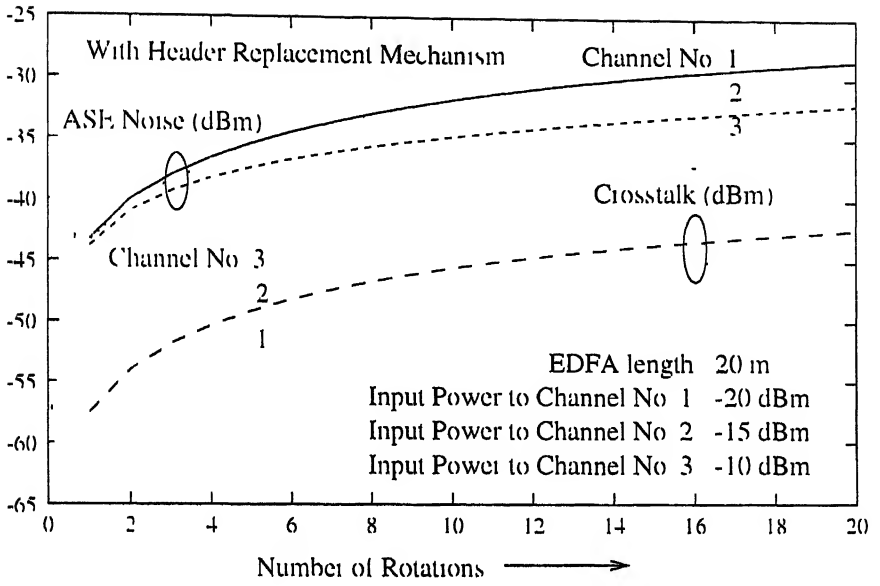


Figure 5.35 ASE noise and Crosstalk noise vs number of rotations for loop with header replacement mechanism for different input power to channels

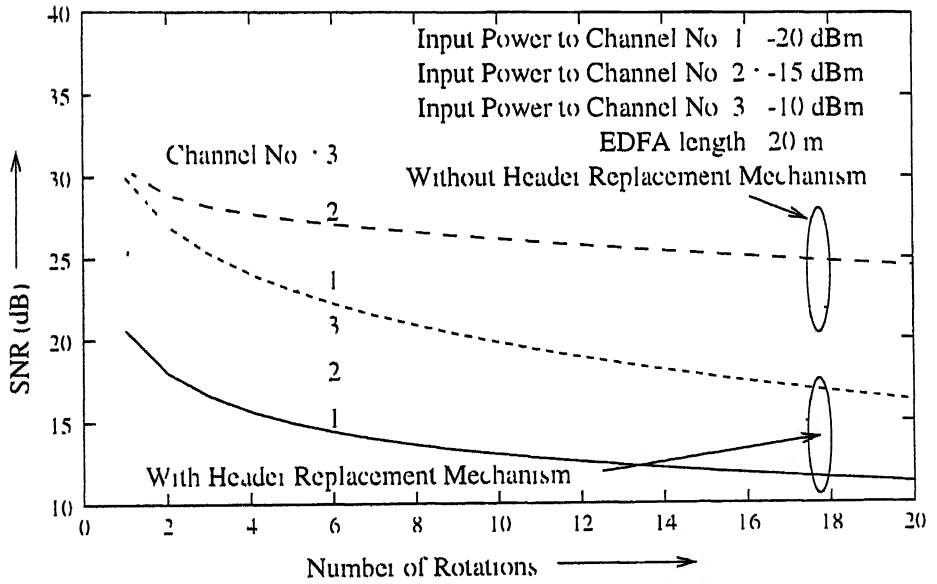


Figure 5.36. SNR vs Number of rotations for loop with and without header replacement mechanism for different input power to channels.

5.4 Conclusion

This work proposes a design to carry out header replacement within an all-optical packet switch. A WDM optical switch based on fiber loop memory has been considered for this purpose. The header replacement is done by using two SOAs in parallel for which a special design of ATM cell having continuous wave as well as guard band is taken. The gain and noise analysis of the switch with and without header replacement mechanism has been carried out using mathematical models.

As discussed in previous Section, the performance of the loop with header replacement mechanism is poor than that of loop without header replacement mechanism. But the loop with header replacement mechanism can be used without any problem for 2, 3 or 4 channels. In general, more than 3 or 4 rotations are not needed for the switch based on FOLM. Hence proposed design can be used suitably not only for 2, 3 or 4 channels but also for 5 channels. The advantage of this design is economical in terms of saving of one SOA for each channel. The loss is in terms of complex control mechanism. Also there is no saving in terms of time. Since every cell will have to make at least one rotation the cells in the proposed design will get delayed by the duration of one cell. While in case of separate header replacement mechanism the delay would be less (equal to that of duration of guard ring and header).

5.5 Future work

As extension of this work, the timing analysis and development of electronic control of the proposed design can be done. Also some assumptions which are made in computational analysis can be done away with. Most important among them is the assumption that packets are input to different channels simultaneously and taken out simultaneously. Computational analysis can be done for the case when packet to different channels are input at different slots and taken out at different slots. Also the loss and crosstalk noise due

to WDM demultiplexer can be incorporated

As further extension of the above problem the computational analysis can be done for several switch connected in succession In fact while developing the computational model (software program) for this thesis work. this issue was considered and the developed model can be easily extended for switches connected in succession

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